Compare Efficiency of Different Multiplier using Verilog Simulation for DSP Application

Anupama A V[1] Bheemashankar[2] Divya K[3] Jagannath[4] Mala Sinnoor[5]
[1,2,3,4]Student [5]Assistant Professor
[1,2,3,4,5]Department of Electronics and Communication Engineering
[1,2,3,4,5]Dr. Ambedkar institute of technology, Bangalore- 56, India

Abstract— The main objective of this project work is to design and simulate simple, appropriate and reliable multipliers for DSP processors. Multipliers are one amongst the foremost important arithmetic units in Microprocessors and DSPs and also a serious supply of power dissipation. Reducing the power dissipation of multipliers could be a key to satisfy the general power consumption of digital circuits and systems. During this paper a High speed and low space design for the Wallace tree using compressed multiplier is projected compared to area architecture. This design is employed in FIR Filter style. The simulation result for eight bit multipliers and 4 tap filters shows that the projected low area and delay architecture lowers the overall area and delay in comparison to array multiplier and Wallace tree using compressed multiplier design based filter. To develop the system blocks in Modelsim 6.4 c and Xilinx ISE13.2.To achieve simulation and synthesis of Spartan3E FPGA tools from Xilinx ISE is employed. Verilog HDL is employed for describing the hardware and system understanding language.
Key words: Multiplier; Adders; Wallace Tree; Xilinx ISE; Reduce Delay, Area and Power

I. INTRODUCTION

The multiplier is a crucial kernel of digital signal processors. As a result of the circuit complexness, the power consumption and area are the 2 vital design issues of the number. During this paper a high speed and low space design. These days each circuit should face the facility consumption issue for each portable device aiming at circuits avoiding cooling packages and dependability problems that are too advanced. It's usually accepted that in logic synthesis power tracks well with space. This suggests that a larger design can usually consume additional power. The number is a crucial kernel of digital signal processor. As a result of the circuit complexness, the facility consumption and space are the 2 vital design thought of multiplier. During this paper a high speed and low area design for Wallace tree using compressed number is planned. For obtaining the high speed and lower area design, the modification created to be standard design carries with it reduction in shift activities of the key blocks of the number, which has the reduction in shift activity of adder and counter. The design is employed in FIR filter style.

The simulation result for 8 bit multipliers and four tap filters shows that the proposed low space, delay and power design lowers the full area and delay in comparison to the array number and Wallace tree using compressed number design primarily based filter. To develop the system blocks in Modelsim 6.4c and Xilinx ISE 14.5. To realize simulation and synthesis of Spartan 3E FPGA tools type Xilinx ISE is employed. Verilog HDL is employed for describing the hardware and system understanding design for the Wallace tree using compressed number is planned for obtaining the high speed and lower area design.

A. FIR Filter

Finite impulse response (FIR) is a basic building block of many digital signal process applications. The FIR filter receives a discrete time signal as input and performs the multiplication and addition operation to present the required filtered discrete time output signal. currently each day several battery operated devices like hearing aids and mobile phones also used FIR filter has it offers stability linear part response as this devices are power hungry devices, a low power FIR implementation is needed for these application.

The FIR implementation is classed as a set co-efficient and programmable filter architectures are completely different from one another.

The FIR filter merely performs the convolution of input with the fastened filter co-efficient. The expression for N-tap filter, it is given as:

$$Y(n) = \sum_{n=0}^{N-1} h(n)x(n-k)$$

B. Wallace tree using compressed technique.

Wallace is a tree of CSA designed for minimum propagation delay. It is enforced by adders using parallel multiplication leading to less delay. Carry save adder methodology is employed so as to reduce the quantity of stages.

The 4:2 compressor structure really compresses the 5 partial product bits into 3. The design is connected in such the simplest way that four of inputs area unit returning from a similar bit position of the burden j whereas one bit is inspired type the neighboring position j-1(known as carry in). The yields of 4:2 blower includes of 1 piece in position j and 2 bits in position j+1. This structure is named compressor since it compresses the four partial products into two.

The block diagram of 4:2 compressor is shown in the figure 1. And compressor design using Full adder is shown in figure 2.

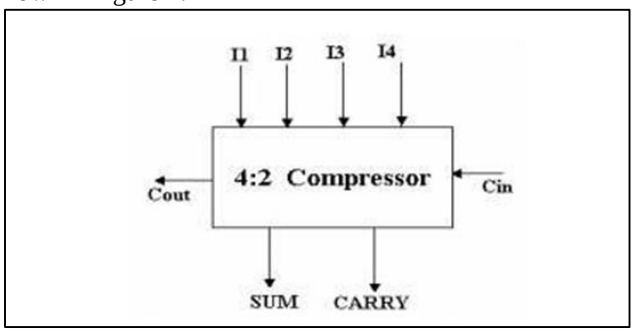

Fig. 1: Block diagram of 4:2 compressor

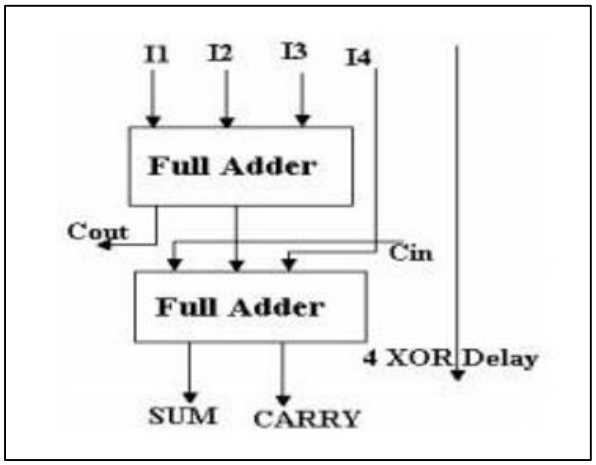

Fig. 2: Compressor design using Full adders

II. BLOCK DIAGRAM OF PROPOSED FIR FILTER

A novel FIR filter structure is so projected to reduce the hardware complexity of the product accumulation blocks. In the projected structure, half the long word-length SA's are replaced by adders, named as pre-structural adders (PSA's) that have comparatively shorter wavelength. We have a tendency to exchange a Wallace tree compressed number rather than array number and shift add number for reducing the delay. The block diagram of a proposed FIR filter is shown in the figure 3.

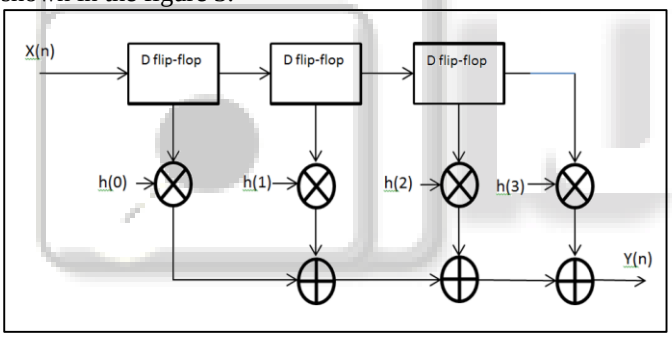

Fig. 3: Block diagram of FIR filter

A. Flip-Flop and Registers.

Flip-flop is a one bit memory cell. The block diagram of D flip-flop is shown in figure 4. D flip-flop is a data flip-flop, which is used for storing the binary bits. To extend the storage capability in terms of range of bits, we've to use a group of flip-flop such a group of flip-flop is thought as register.

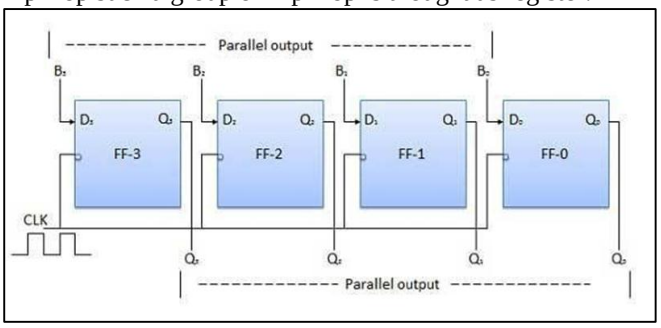

Fig. 4: Block diagram of D Flip-Flop

B. Algorithm proposed.

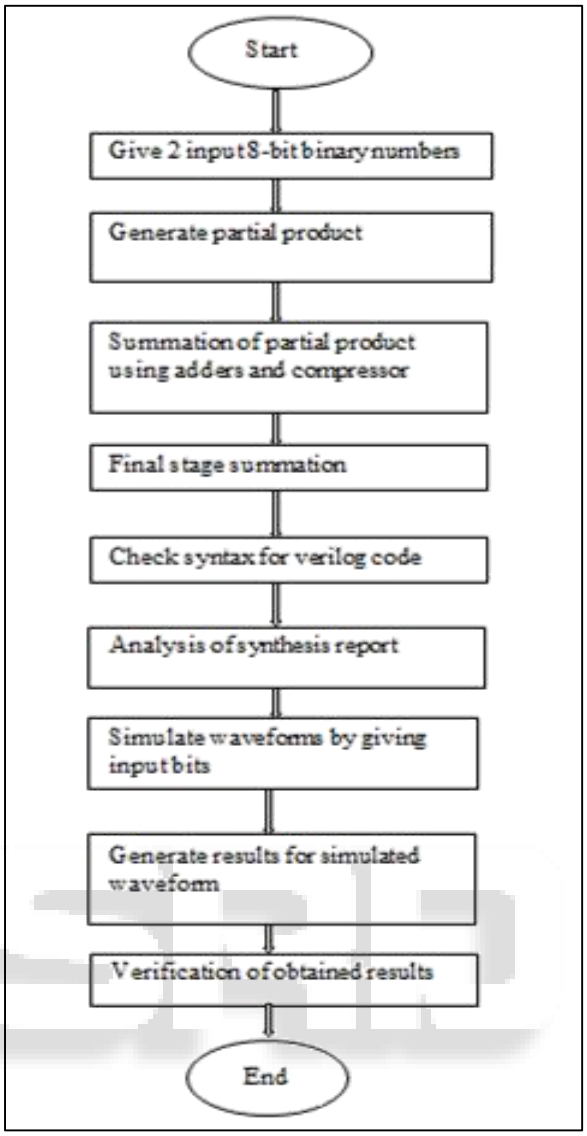

Fig. 5: Proposed algorithm of Wallace tree using compressor technique

III. METHODOLOGY

Verilog HDL is a hardware description language (HDL). It is used to describe digital system. HDL would possibly describe the layout of wires, resistor, and transistor on integrated circuit chip, i.e., and therefore the switch level. Or, it would describe the logical gate and flip-flops i.e., gate level. An excellent higher level describes the register and therefore the transfer vector of data between register, this is often known as the register transfer level (RTL).

Verilog is one among the 2 major hardware description languages utilized by hardware designer business and domain, VHDL is another one. The industry presently split on that is healthier several feel that Verilog is simpler to find out and helpful than VHDL.

IV. RESULT AND ANALYSIS

In this paper implementation and result of 8 bit array multiplier using Xilinx ISE 14.5 are discussed. The FIR filter with wallace tree multiplier have been designed and analyzed with the performance parameters.

Fig. 6: Main RTL schematic

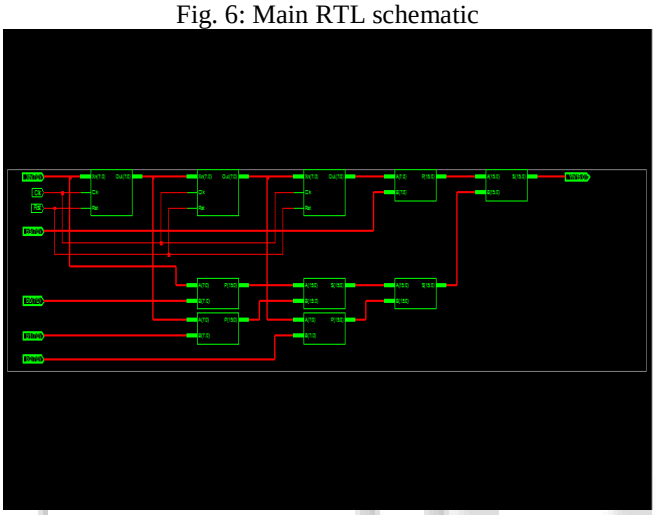

Fig. 7: FIR filter based on wallace tree

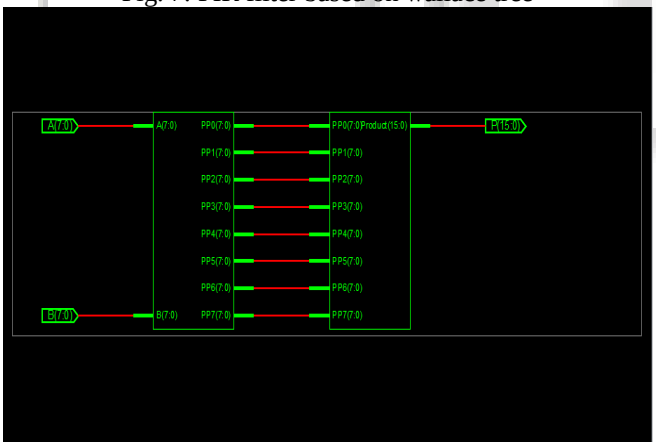

Fig. 8: Wallace tree multiplier based on compressor

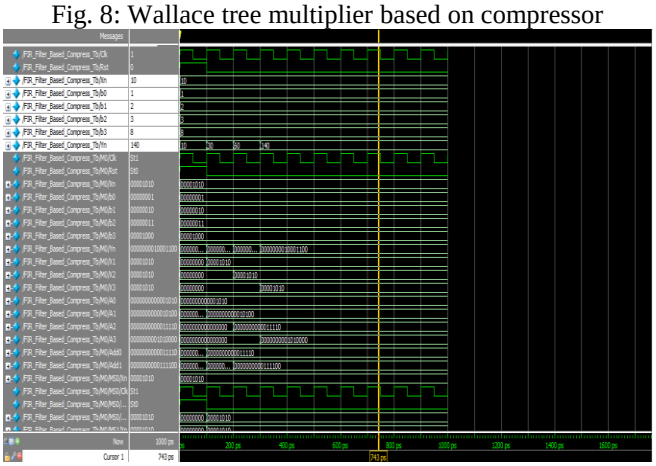

Fig. 9: FIR filter based on wallace tree using compressed Multiplier

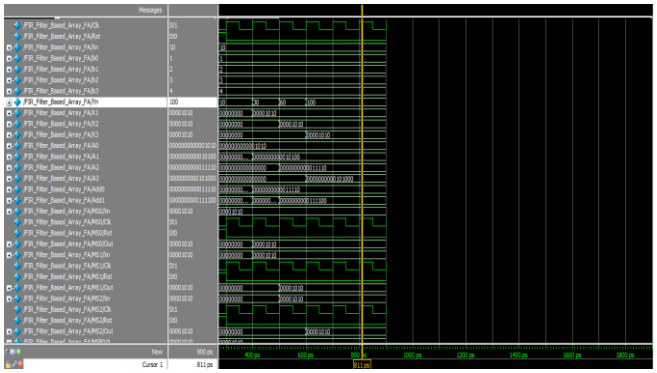

Fig. 10: FIR filter based on Array multiplier(FA)

V. COMPARISION TABLE

The below table shows the area, delay and power consumption of Wallace tree using compressor is less compared to array multiplier using Full adders.

Device Name	Area			Delay			Power
FPGA Spartan 3 XC 3S 5000 FG 900 -4	Slices	LUT	Gate	Delay	Gate Delay	Path Delay	Power consumption
Wallace Tree using Compressed Multiplier	362	638	4,032	36.805ns	16.912ns	19.893ns	0.852w
Normal Multiplier using FA	394	698	4,398	39.108ns	17.463ns	21.645ns	1.483w

VI. CONCLUSION

The projected design area and delay efficiency and power consumption in comparison to a Wallace tree using compressed multiplier and array multiplier, the proposed architecture makes use of bit dimension management logic and low area and Delay. This design is used in FIR filter design. The simulation result for 8-bit multipliers and 4-tap filters shows that the proposed low area and Delay architecture lowers the entire area, delay and power consumption in comparison to the array multiplier and Wallace tree using compressed multiplier architecture primarily based filter. The design will be verified using Modelsim with Verilog HDL code and area and delay is analysed using Xilinx ISE software. From the table and comparison graph, proposed design can attend less area, less delay and less power consumption in comparison to the conventional array multiplier and Wallace tree using compressed multiplier.

REFERENCES

[1] A.Chandrakasan and R. Brodersen, “Low Power CMOS Digital Design”, IEEE J. Solid State Circuits, Vol.27, no.4, pp 473-484, Apr 1992

[2] N.Y.Shen and O.T.C.Chen."Low power multipliers by minimizing switching activities of partial products" in Proc. IEEE Int.Symp.Circuits Syst., May 2002, Vol.4, pp 93-96.

[3] O.T.Chen, S.Wang and Y, W.Wu "Minimization of switching activities of partial products for designing low power multipliers" IEEE Trans. Very Large Scale

Integer .(VLSI)Syst. , Vol .11, No-3, pp418-433, June 2003

[4] B.Parhami Computer arithmetic algorithms and Hardware designs 1 st ed.Oxford U.K. Oxford Univ, Press 2000.

[5] K.H.Chen and Y.S.Chu , "A low power multiplier with spurious power suppression technique" , IEEE Trans. Very Large Scale Integr .(VLSI)Syst. , Vol.15 , no-7,pp846850, July 2007.

[6] K.H.Chen K.C.Chao,J.I.Guo,J.S.Wang and Y,S,Chu. "An efficient spurious power suppression technique (SPST) and its applications on MPEG-4 AVC/H.264 transform coding design" in Proc.IEEE Int.Symp.Low Power Electron.Des . 2005 pp 155-160

[7] M.Mottaghi Dastjerdi ,A.afzali Kusha,m.Pedram "BZFAD A Low Power Low Area Multiplier Based on Wallace Tree using Compressed Architecture " IEEE Trans. Very Large Scale Integr .(VLSI)Syst., Vol.17, no-2,pp302-306, Feb. 2009

