A Review on Error Tolerant Adder for DSP Applications

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Abstract— In today's world as the technology is enhancing, all the errors that occurs in the system must be handle on the priority. As the VLSI deals with fast and accurate results error tolerant adder are in used according to the requirement in different DSP applications. This type of adder provides an alternative to use simple adder or error tolerant adder, by using such devices low power consumption, high speed and small area can be achieved. As the application require accurate result it will use accurate adder or simple adder but if the application my tolerate some error in that case ETA is used to reduce the above mentioned parameters.

Keywords: Adders, Digital Signal Processing (DSP), Error Tolerance, Low-Power Design, VLSI

I. INTRODUCTION

In the recent year, there is influx of large portable devices that performs several functions of multimedia. The energy efficiency is the prime concern for these portable devices and user cannot withstand rapid discharge of battery rather can manage with lower performance/quality. The large power consumption in these portable devices increases the failure probability which may result in device burnout/hanging-out etc. The conventional approaches to achieve efficient design is the scaling where devices size along with supply are reduce with the same factor. But, the scaling has reached to the point where further scaling may result in process and other variation that degrades the performance of these devices significantly. Hence scaling the device dimension fails to achieve energy efficient design. So the design of low-power and high speed VLSI architectures needs efficient arithmetic processing units which are optimized for the performance parameters, namely, speed and power consumption. For any general purpose microprocessors and DSP processors adders are the key components. It is also used for division, and multiplication purpose and adder is measured by their speed performance.

In modern VLSI design, it is evident that errors occur everywhere ranging from design to verification. So, for these applications an emerging concept is proposed error tolerance, ET [1],[2]. These designs deal with error tolerant circuits. By the definition, a circuit is error tolerant if: it contains defects that cause internal and may cause external errors and the system that incorporates this circuit produces acceptable results. The energy efficient design is the prime challenge for the latest VLSI technology which is required by modern portable devices due to increased functionality on the single chip. The energy efficiency can be achieved through designing circuit imprecisely.

Moreover, the complexity of the devices is increasing exponentially due to increased functionality. All the circuits on these portable devices demand highly energy efficient designs as user cannot tolerate the fast discharge of battery [3]. The energy efficient designs not only increase the battery lifetime but also increases the reliability of the system. Not all digital systems have errors but some digital system like control systems output there is always needs correct signal so, eliminate the use of error tolerant adders. Moreover, for many DSP systems that process signals related to human senses- hearing, smell, eye sight, and touch are always engaged with some errors and also in the multimedia applications such as- the image and video processing systems, are always deals with minor errors [3], [4], and [5]. So for these applications error tolerant adder is used in the design of approximate architectures that provides almost correct results at improved design metrics [6]. Hence, we can improve all the design parameter simultaneously at minor loss in accuracy by approximate designs. On the other hand, the designing of an accurate circuit by error tolerant circuit is the totally waste of power, area and performance.

II. ERROR-TOLERANT ADDER

Some terminologies used to define error tolerant adder are given below:

– Overall error (OE): It is define as the difference between correct answer and result obtained by the adder

$OE=|R_C-R_e|$

Where R_e is the result obtained by the adder, and R_C denotes the correct result (all the results are represented as decimal numbers).

– Accuracy (ACC): In case of the error-tolerant design, the accuracy of an adder is used to indicate how "correct" the output of an adder is for a particular input. It is defined as:

$ACC = (1-(OE/ R_C)) X100\%.$

Its value ranges from 0% to 100%.

– Minimum acceptable accuracy (MAA): Although some errors are allowed to exist at the output of an ETA, the accuracy of an acceptable output should be "high enough" (higher than a threshold value) to meet the requirement of the whole system. Minimum acceptable accuracy is just that threshold value. The result obtained whose accuracy is higher than the minimum acceptable accuracy is called acceptable result.

– Acceptance probability (AP): Acceptance probability is the probability that the accuracy of an adder is higher than the minimum acceptable accuracy. It can be expressed as:

AP = P (ACC>MAA), with its value ranging from 0to 1.

A. Need for Error-Tolerant adder

Increasingly huge data sets and the need for instant response require the adder to be large and fast. Because of low-speed performance of traditional ripple-carry adder (RCA) ,it is not suitable for large adders. Many different types of fast adders, such as the carry-skip adder (CSK) [7], carry-select adder (CSL) [8], and carry-look-ahead adder (CLA) [9], have been developed. Also, there are many low-power adder design techniques that have been proposed [10]. However, there are always trade-offs between speed and power. There is solution of above mention problem; the error-tolerant design will be the best solution. By sacrificing some accuracy, the ETA can

attain great improvement in both the power consumption and speed performance.

III. LITERATURE REVIEW

Error Tolerant Adder-I (ETA-I)
The logic and working principle of the ETA-I is discussed in the following subsections [11].

A. Logic for ETA-I

The working principle of the ETA can be better understood via an example as shown in Figure 1. In this, we take two 16-bit input data as, X= "1011001110011010" (45978) and Y= "0110100100010011" (26899). Initially entire input bits are divided into two parts: namely higher order accurate part whereas least significant bit makes a lower part. The addition mechanism starts from the joining point towards the two opposite directions simultaneously. For the accurate part normal addition is applied from right to left to preserve its correctness and for inaccurate part no carry signal will be generated. To reduce the amount of error in the overall addition an approximation method is utilized in the approximate part in which carry will not be generated and forward. For inaccurate part and can be described as follows: i) check every bit position from left to right (MSB to LSB); ii) If both input bits are "0" or different, normal one-bit addition is applied and the operation proceeds to next bit position; iii) If both input bits are "1", the checking process stopped and from this bit onwards, all sum bits to the right are set to "1" as shown in Figure 1 with a final result of "10001110010011111" (72863). The example given in Figure 1 should actually yield "10001110010101101" (72877) if normal arithmetic has been applied. The overall error is OE = 72877−72863 = 14. The accuracy of the adder with respect to these two input bits is ACC = (1− (14 / 72877)) ×100% = 99.98%. Thus, the ETA reduces the delay by nearly half.

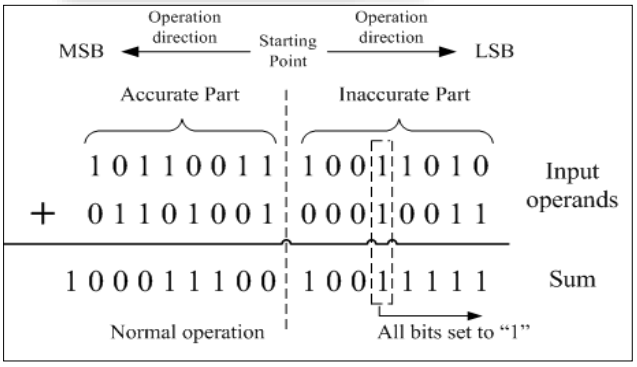

Fig. 1: Error Tolerant Adder [11]

B. ETA-I Architecture

The architecture diagram of the ETA is shown in the Figure 2, which shows that error tolerant adder (ETA-I) is divided in two parts: accurate part and inaccurate part. The accurate part includes higher order bits and the inaccurate part includes remaining lower order bits. Since the higher order bits play more important role than the lower order bit normal addition method is applied for accurate part to preserve its correctness and special strategy is adopted for the inaccurate part. Further its accurate part is implemented with any of conventional adder such as the RCA, CSK, CSL, or CLA. Its carry is grounded and the accuracy of accurate part is too strong. Another side the inaccurate part is implemented with the combination of two blocks; a control block and a carry free addition block. The control block is made up by and-or logic to generate the control signals, for the working mode of the carry free addition block. And the carry free addition block is made up by modified XOR gate where three extra transistors are added to a conventional XOR circuit and with additional control signal. Both accurate as well as inaccurate part discussed further in the following subsections.

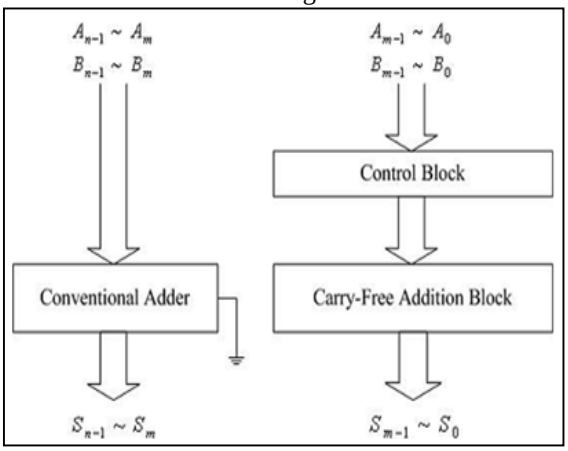

Fig. 2: Architecture diagram of ETA [11]

32-bit adder is used here as an example for our illustration design of an ETA. It contains two parts namely design of accurate and inaccurate part which is follows:

1) Design of Accurate Architecture

When we design our 32-bit ETA then accurate part is made up of 16-bit. Since the overall delay depends on the worst case delay of the accurate or approximate part, fast adder for accurate part may results in less delay. So the ripple carry adder, which is the vastly power-saving conventional adder, used for the accurate part.

2) Design of Inaccurate Architecture

The inaccurate part can be divided in two blocks on which generates the control signal while the other that will provide the approximate sum. This approximate sum logic can be build using 16 modified XOR gates, and each of which is used to generate a sum bit. The block diagram of modified XOR gate with external control input is presented in Figure 3 the external control input is coming from Figure 5. The modified XOR gate is also known as MXOR. And all the additions are performed by modified XOR circuit.

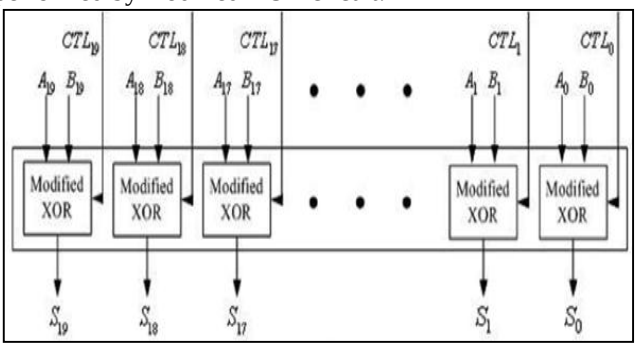

Fig. 3: Architecture diagram of carry free addition block [11]

The circuit diagram of the modified XOR gate as shown in Figure 3.8 illustrate that modified XOR requires 5

addition transistors. In the circuit CTL is the control signal given by the control block and determines the output sum value. In case of CTL= 1, the XOR gets disconnected and the output is set to logic 1. Whine in case of CTL =0, XOR simply provides the addition of two inputs A and B.

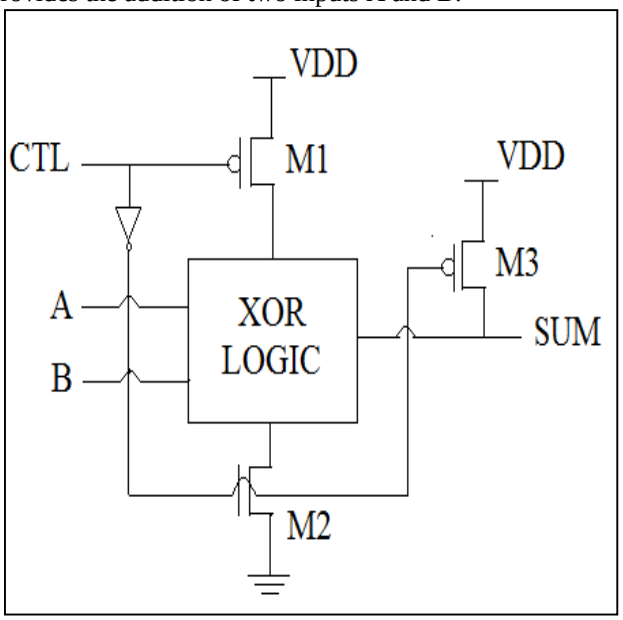

Fig. 4: Schematic diagram of modified XOR gate [11]

The control block uses AND-OR logic. The control block is shown in Figure 5, which takes input and execute then generates the control signal and output for each block of the modified XOR gate as input.

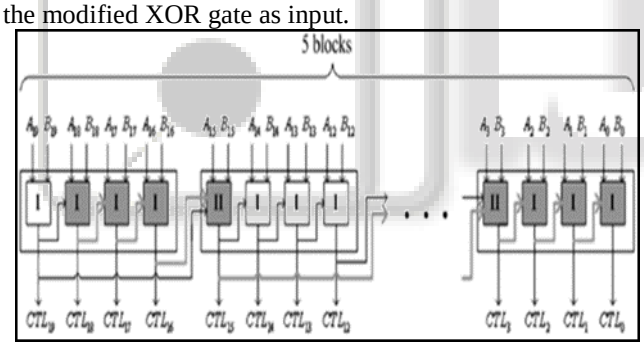

Fig. 5: Architecture diagram of control block [11]

3) ETA-II Adder

Zing et al. [7] introduced an error tolerant adder ETA-II which is different from ETA-I, as ETA-II does not divide the input two parts and does not exhibits completely approximate logic for the non-significant part. ETA-II segments input into several sub-adder and computes the sum of each sub-adder in accurate manner i.e. ETA-II design curtails the carry propagation to few bits to eliminate the long carry propagation path of the accurate adder. The reduced carry propagation path significantly improves the performance of the adder. The architecture of the ETA-II is shown in Figure 6 where it utilizes sum generator to compute the sum of partial bits of the operands and carry generator to compute the carry in for the sub-sequent sum generator.

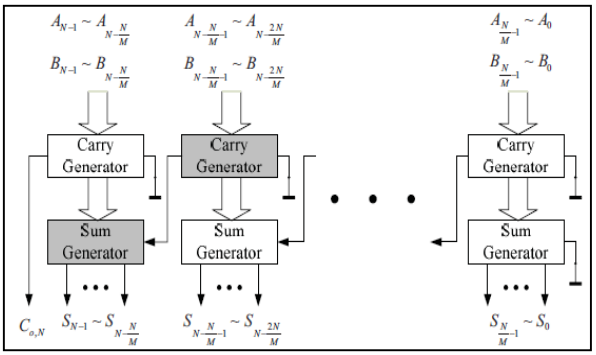

Fig. 3.6: Circuit diagram of the ETA-II adder.

Consider the addition process of binary number, the carry signal at each bit position is determined by the previous input bits. For the worst case, this carry signal is generated at the LSB and propagates along the carry chain to the current bit position. If this worst case happens, significant power consumption and delay overhead will occur due to the long carry propagation. But in fact, the worst case seldom happens. For most of the cases, this carry signal can be determined by just several input bits on the right of the current bit position. Assume that the input operands are perfectly random; the probabilities of getting correct carry signal on any bit when different number of bit positions to the right is involved in determining the carry signal can be derived.

From the literature review it is observed that the performance of the error tolerant adders can be further improved. The proposed work focuses to achieve an approximate adder that provides improved performance over these existing approximate adders.

IV. Conclusion

In VLSI design the new concept is introduced, error tolerance design. It is designed according to the requirement. If accuracy is needed the novel type of adder is used and if the error is tolerated error-tolerant adder is used. By using this type of adder which trades certain amount of accuracy for significant power saving and performance improvement, is proposed. On comparisons conventional digital adders and the proposed ETA showed that, proposed ETA outperforms the conventional adders in both power consumption and speed performance.

The main applications of the ETA were areas are no strict requirement on accuracy or where super low power consumption and high-speed performance are more important than accuracy. One of the best applications is in the DSP application for portable devices such as cell phones and laptops.

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