FPGA Implementation of Decimation Filter using Canonic Signed Method

Ku. Rupali B. Sawai[1] Dr. R. M. Deshmukh[2]
[1]M.E. Student [2]Head of Department
[1,2]Department of Electronics & Telecommunication Engineering
[1,2]Dr. RGIT&R, Amravati, India

Abstract— The hearing aid decimation filter is one of the technique employed with the help of FPGA simulation in which the problems of hearing loss person are considered and provides a better solution for hearing aid in quite as well as in whisper conditions for clear hearing. The design of decimator filter requires a set of filters for hearing aid applications that gives reasonable signal for the concerned type of hearing loss. Using a variable bandwidth filter, helps a person with hearing loss to listen and communicate by making sounds audible and clearer. The design of variable bandwidth filter is carried out for gain, such that, the different bands combine to give a frequency response that closely matches with audiogram. The technique employed for the design of the filter is Canonic Signed Digit (CSD) representation. The higher sampling rate of the signal is decimated to low sampling rate by implementing the filter using the multi rate a set of selected bandwidths. The main aim of the paper is to analyse and simulate the decimation filter using MATLAB. It is then simulated with ISE software to analyse a frequency response of a filter at particular level of frequency. Minimum frequency of a person hearing is usually considered to be 20 Hz whereas the maximum limit is 20 kHz, but the ear is more sensible to audio from 1 KHz to 4 KHz. Thus, it is beneficial to design a deaf aid application that operates in the desired range of frequency and makes use of oversampling concept.

Key words: Decimation Filter, CIC Filter, FIR Filter, FPGA, Half Band Filter, MATLAB, Xilinx

I. INTRODUCTION

A hearing aid is helpful for the people having hearing loss to hear more precisely in both quiet and whirring situations. It helps a person with hearing loss to listen and communicate by making sounds audible and clearer. The technique employed for the design of the filter is Canonic Signed Digit (CSD) representation. The higher sampling rate of the signal is decimated to low sampling rate by implementing the filter using the multi-rate approach.

The concept of over sampling the analog-to-digital conversion is very common to achieve the enhanced performance and flexibility. Apparently, the perfect reconstruction of bandwidth-limited signal is possible if it is sampled at or above the Nyquist frequency. The minimum frequency of a person hearing is usually considered tobe20Hzwhereasthe maximum limit is 20 kHz, but the ear is more sensible to audio from1KHzto4KHz. Thus, it is beneficial to design a deaf aid application that operates in the desired range of frequency and make sure of oversampling concept.

A Field Programmable Gate Arrays or FPGAs are based around a matrix of configurable logic blocks [CLBs]. It is an integrated circuit that may be programmed or reprogrammed to the desired capability or software after manufacturing. Important characteristics of field-programmable gate arrays consist lower complexity, higher speed, programmable functions and volume designs. Nowadays, FPGAs as cost effective integrated tools have any applications in the field of communication and a growing range of other areas. Using FPGAs for hardware acceleration in software defined radios (SDR) offers extensive processing power to realize promised portability of waveforms and re-configurability. The decimation process requires a low-pass filter of high quality and a sampling rate converter that helps to reduce the sampling frequency to a low level.decimation filter (decimator) is one of the basic building blocks of a sampling rate conversion system. The decimation filter performs two types of operations: low-pass filtering as well as down sampling. The filter converts low resolution high bit-rate data to high resolution low frequency data. It is mostly used in such applications as speech processing, radar systems, antenna systems and communication systems. Considerable attention has been focused in the previous years on the design of high efficiency decimation filters. The decimation process requires a low-pass filter of high quality and a sampling rate converter that helps to reduce the sampling frequency to a low level. A hearing aid is helpful for the people having hearing loss to hear more precisely in both quiet and whispering situations.

II. LITERATURE REVIEW

A hearing aid is helpful for the people having hearing loss to hear more precisely in both quiet and whirring situations. It helps a person with hearing loss to listen and communicate by making sounds audible and clearer.K. Grover[1], Proposed the technique employed for the design of the filter is Canonic Signed Digit (CSD) representation. The higher sampling rate of the signal is decimated to low sampling rate by implementing the filter using the multi-rate approach. The main aim of the paper is to analyze and simulate the decimation filter using MATLAB. It is then simulated with ISE and finally implemented on FPGA devices. The comparison is done on two filter structures, Direct-form FIR and Direct–Form Symmetric FIR, for hardware resource utilization and speed. The designed FIR filter with symmetric structure designed on Virtex2P displays effective utilization of area and better speed in comparison to the design with Direct-Form structure on Spartan3E.

The design of decimator filter requires a set of filters for hearing aid applications that gives reasonable signal for the concerned type of hearing loss. Using a variable bandwidth filter, helps a person with hearing loss to listen and communicate by making sounds audible and clearer. The design of variable bandwidth filter is carried out for a set of selected bandwidths. Each of these bands is frequency shifted and provided with sufficient magnitude gain, such that, the

different bands combine to give a frequency response that closely matches with audiogram. T. Rahate [2] Proposed the technique employed for the design of the filter is Canonic Signed Digit (CSD) representation. The higher sampling rate of the signal is decimated to low sampling rate by implementing the filter using the multi rate approach. The two FPGA devices can be used Spartan-3E and Virtex2Pro. Furthermore, multi rate filtering method is used to attain high-resolution. It may reduce the complexity of the circuit and also the overall power consumed.

From the last few years, there has been a vast growth in the field of VLSI, Optimized decimation filters for wireless communication receivers based on FPGA is use by Vennached Karunakeroud [3], concluded poly phase required more area in comparison with CIC based filter and for both the decimation and interpolation, CIC filters are used multirate digital signal processing.

Number of signal processing algorithm have been developed by Siddharth Raghuvanshi [4], which allow the user to focusing on real time signals such as speech to convert the signal with desired quality. The digital hearing aids are performed on Application Specific Integrated Circuit (ASIC) , not only the efficiency and complexity of Hearing aid increases but also required more space and because implementation of hearing aid in digital is not interesting task and more power consuming also on ASIC.

Divya Naga Padmini P [5] represents different ways of realizing half-band FIR low pass filter and provides comparison of critical path delay and clock frequencies for direct form, transposed form and DA (Distributed Arithmetic) type of architectures, In this paper, because of using multipliers which gives rise to few demerits in terms of increase in area and increase in the delay which ultimately results in less performance. To resolve this issue, DAA (Distributed Arithmetic Architecture) is used which is a popular method for implementing digital FIR filters on FPGAs through which delay can be reduced and multiplier less realization can be achieved.

III. PROPOSED WORK

A Field Programmable Gate Arrays or FPGAs are semiconductor devices that are based around a matrix of configurable logic blocks (CLBs). It is an integrated circuit that can be programmed or reprogrammed to the required functionality or application after manufacturing. Important characteristics of field-programmable gate arrays include lower complexity, higher speed, programmable functions and volume designs. Nowadays, FPGAs as cost-effective integrated tools have many applications in the field of communication and a growing range of other areas. Using FPGAs for hardware acceleration in software defined radios (SDR) offers extensive processing power to realize promised portability of waveforms and re-configurability. The decimation filter (decimator) is one of the basic building blocks of a sampling rate conversion system. The decimation filter performs two types of operations: low-pass filtering as well as down sampling. The filter converts low resolution high bit-rate data to high resolution low frequency data. It has been widely used in such applications as speech processing, radar systems, antenna systems and communication systems. Considerable attention has been focused in the last few years on the design of high efficiency decimation filters. The decimation process requires a low-pass filter of high quality and a sampling rate converter that helps to reduce the sampling frequency to a low level. A hearing aid is helpful for the people having hearing loss to hear more precisely in both quiet and whirring situations.

It helps a person with hearing loss to listen and communicate by making sounds audible and clearer. The minimum frequency of a person hearing is usually considered to be 20 Hz whereas the maximum limit is 20 kHz, but the ear is more sensible to audio from 1 KHz to 4 KHz. Thus, it is beneficial to design a deaf aid application that operates in the desired range of frequency and makes use of oversampling concept. Furthermore, multi rate filtering method is used to attain high-resolution. It can reduce the complexity of the circuit and also the overall power consumed. There are two important parameters which effects hearing. One is loudness that is the intensity of sound and the other one is pitch, which is the frequency of the fundamental component in the sound.

A. Hearing Aid Concept:

Digital Hearing Aid process the speech signal in the same manner as human ear functions. Human ear has three main part outer ear, middle ear and inner ear. Outer ear receives the signal from outside world and direct towards the middle ear, in Digital Hearing Aid directional microphone performs this task. Middle ear acts as an impedance matching network and as an amplifier. Main function which middle ear performs is the distribution of frequency bands into several small bands. Digital Hearing Aid uses some kind of impedance matching network along with the amplifier. Signal processing algorithms such as DFFT, FFT, Uniform or Non-Uniform filter bank is implemented on FPGA to split the entire frequency band into several small bands so that desired band of frequency can be manipulated as per the need of patient.

We have to develop Decimator filter (FIR Filter) based on FPGA. but for known output frequency response (sensitive to hearing aid person), first we have to find its frequency coefficient. So first will develop code in MATLAB to find its coefficient for CIC Decimator Filter. Later after getting coefficient, we'll develop and compare FIR filter architectures i.e. Direct Form and Direct Symmetric as per base paper and compare its result with respect to FPGA device in Xilinx ISE or Intel Quartus2 platform. There is no hardware i.e. FPGA implementation on FPGA kit, its only architecture analysis project.

This circuit requires analog to digital converters (ADC) of high speed and high resolution. The decimation process requires a low-pass filter of high quality and a sampling rate converter that helps to reduce the sampling frequency to a low level. It is evident from the block diagram that initially, the input is sent from the microphone. Then, the preamplifier and AGC are used to amplify the signal. After that, sigma delta modulators are designed to shape the noise away from the undesired band. The desired frequency is then transferred to the decimator.

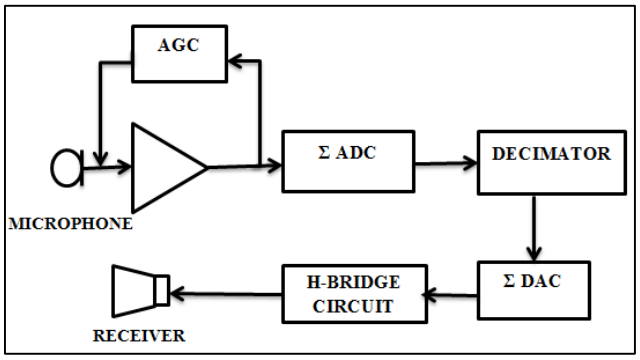

Fig. 1: Proposed circuit

The H-Bridge driver circuit is used in the front end of receiver. Furthermore, multi-rate filtering method is used to attain high-resolution. It can reduce the complexity of the circuit and also the overall power consumed. Also, comb filters are used at the beginning stage of the decimation filter in this approach. In this paper, the proposed architecture is designed to reduce the hardware requirement and the power consumption. A comb half band FIR-FIR structure is implemented and it is designed using canonic signed digit representation, which leads to reduced hardware complexity and less consumption of power in comparison to other decimation filters.

1) The CIC Filter: The sampling rate is converted from low to high is called a cascaded integrator comb (CIC) filter. The comb filters do not need any multipliers and hence includes simple functions that are desirable at high frequencies. The response of the comb filter is a low pass filter with a distinct cutoff.
2) Design half band FIR filter: Half-band filter is a fundamental building block in multi rate signal processing. Half-band filters are mostly used for their efficiency in multi-rate applications. The two important characteristics of Half band filters are pass band and stop band, the ripples of these band must be the same, and the pass band-edge and stop band-edge frequencies are equal distance from the half band frequency.
3) Using Corrector Filter: Corrector filter is used for removing the unwanted signals. Digital filters with finite duration impulse response (all-zero, or FIR filters) have the advantages are exactly linear phase, always stable as well as the filter start up transients have finite duration.

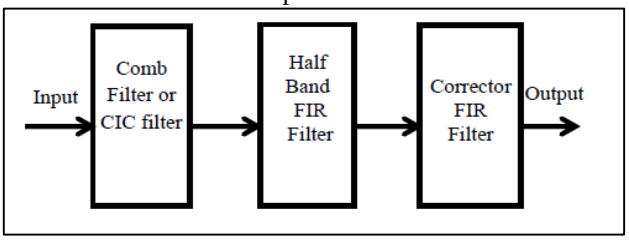

Fig. 2: Block diagram of decimation filter

In digital signal processing down-sampling and decimation are terms associated with the process of re-sampling in a multi-rate digital signal processing system. Both terms are used by various authors to describe the entire process, which includes low-pass filtering, or just the part of the process that does not include filtering. When down-sampling (decimation) is performed on a sequence of samples of a signal or other continuous function, it produces an approximation of the sequence that would have been obtained by sampling the signal at a lower rate (or density, as in the case of a photograph). The decimation factor is usually an integer or a rational fraction greater than one. This factor multiplies the sampling interval or, equivalently, divides the sampling rate. For example, if compact disc audio at 44,100 samples/second is decimated by a factor of 5/4, the resulting sample rate is 35,280. A system component that performs decimation is called a decimator.

At a time of designing or creating a decimation filter, firstly decided which type of filters will be used for perfect getting output as well as where decimation will occur. For implementing the proposed structure and design flow for decimator filter implementation are as follows:

1) Define the filter specifications such as order, filter design, cut-off frequency, differential delay, pass band ripple and sampling frequency.
2) Calculate the filter coefficient and stimulate in MATLAB environment and then model Simulink performed.

B. Simulation

On the basis of the simulation results the whole system may be implementing in software using the Xilinx or Quartus II. Xilinx ISE (Integrated Synthesis Environment) is a software tool produced by Xilinx for analysis, stimulate a design's reaction to different stimuli, perform timing analysis and configure the target device with the programmer. Quartus II is programmable logic device design software produced by Altera, before Altera was acquired by Intel and the tool was renamed to Intel Quartus II enables analysis as well as synthesis of HDL designs, which enables the developer to compile their designs, perform timing analysis, stimulate a design's reaction to different stimuli, and configure the target device with the programmer.

After design of filter code in MATLAB FDA tool we get a filter coefficients which is of the frequency format of normal signal frequency which is comes from the sender towards the hearing aid person. After getting this frequency component or coefficient we compare this factor with the referenced frequency factor which is in the range of 1KHz to 4KHz which is more sensible to human ear. This frequency range factor are obtained in the Xillinx software in the form of matrix by coding technique. Which is after implemented on FPGA devices. After comparing only desired frequency will be transmitted and remaining are blocked. And hence desired output with high gain is achieved. And this is found with the help of signal analysis in software tool which is nothing but the aim of this project.

IV. ADVANTAGES

- It is give a signal response in whispering as well as quit situation.
- This is cost effective system and gives output at quite as well as whispering condition.

V. APPLICATIONS

- Used in Military, Forensic area etc.

- For amplify the signal and also reduce the sampling frequency to a low level.
- A hearing aid is helpful for the people having hearing loss to hear more precisely in both quiet and whirring situations

VI. CONCLUSION

As we proposed a system to an efficient method for the design of digital filters suitable for digital hearing aid. The higher sampling rate of the signal is decimated to low sampling rate by implementing the filter using the multi rate approach. The decimation filter gives better results in terms of speed, timing analysis, efficiency and resource utilization etc. Specifications of decimator filter such as ripple factor, number of stages, pass band frequency, cut off frequency, Differential delay etc. will finding on the bases of filters after simulation. Cascading several multi rate stages increases the design efficiency, which reduces the total number of coefficients and in turn results in hardware savings and also less power consumptions. This all analysis will be observed in the respective software tool for respective Frequency response.

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