A Novel Design of Self-Start Counters using Reversible Gates

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Abstract— When Moore's law comes to the end, reversible logic is considered as the most promising technology to solve the problem of high power dissipation. Among the applications of reversible logic, quantum computing is one of the most significant issues in that the nature of quantum mechanics is reversible. Now many researchers concentrate their efforts on designing reversible circuits. One of the basic elements in the reversible sequential circuit is counter. In this paper, we proposed a novel design of a reversible counter whose chief characteristic is self-starting. Unlike other regular reversible counter designs, we fully consider the circumstance when reversible counter enters the invalid states, and we will make sure that the counter can still count even enters the invalid states. In addition, we also deal well with the irreversible problem brought by self-starting, and it should be noted that the design method of the self-start counter is different from the regular reversible counters which are just simply replaced with reversible gates directly. We presented a detailed analysis of a MOD-7 counter with self-starting character in this paper.

Keywords: Reversible logic, Quantum computing, Self-start counter, Invalid states

I. INTRODUCTION

Moore's law predicts that the size of the silicon-based chip will reach limitation, and the problem with that is higher power dissipation and the heat accumulating in the chip will cause the circuit to burn down. Landauer's principle[1] has proved that erase one bit of information will release at least $kT \ln 2$ joules energy. The dissipation energy is related to the lost information bits. For example, an AND gate has two inputs but with only one output, which means that in the process of signal transmission from input to output, one bit of information lost and this is the main reason to cause the power dissipation. Hence, the total heat of the chip will increase evidently with the size, and low power dissipation becomes an important issue for VLSI design. Fortunately, Landauer's law also shows that the reversible logic circuit can achieve zero energy dissipation theoretically as it doesn't lose information during the computation. The reversible logic circuit is considered as the most efficient method to solve the problem of the power dissipation. Bennett demonstrated that almost every computation operations can be carried out in a reversible way, not only in logic level but also in physical level[2]. Many researchers focus their study on reversible logic applied in many other fields like quantum computing and optical computing, etc. And in the long run, quantum computing is a superior future technology since the quantum operation is reversible in nature, the research on reversible logic has promoted the development of the quantum computer.

Nowadays, much work has been done in the area of reversible logic circuits, and a certain number of scholars are studying the design of reversible circuits containing combinational logic circuits and sequential logic circuits. Several elementary reversible gates composed of the primitive quantum gates such as Toffoli gate[3], Feynman gate[4] and Fredkin gate[5], etc, have been built. Picton firstly proposed the basic reversible model of Latch [6], and after that, various reversible sequential circuits[7,8] had been put forward. Thapiyal proposed several elementary reversible flip-flops like D flip-flop and RS flip-flop and so on[9]. Some application circuits such as shift register[10,11] and counter[12,13] based on these reversible gates were also built. Among these application circuits, counter is one of the most widely used sequential circuits.

There exist some designs of the reversible counter, but most of which are designed normally with no consideration about the redundant states or just avert the redundant states. In fact, the counter may fail to work if entering the invalid states. We have to consider the circumstance when the counter enters the failure mode because of the invalid states and how we can make the reversible counter work properly even in the invalid states. When we design the self-start counter, in particular, what we should pay more attention to is the reversible issue as well as the difference between the reversible design and the classical non-reversible counter design.

In this paper, we propose a novel design of a reversible counter via the state transition diagram and truth table with full consideration of the invalid states. For irreversible problem the self-start design brings, we present a novel method to design a reversible circuit, as compared with the regular design method proposed in other papers.

In section 2, we will describe the background of relevant basic concepts about reversible gates and some previous works about the designing of regular reversible counters. Section 3 proposes an idea of constructing a self-start counter using reversible gates and gives a detailed illustration with an example of MOD-7 counter which has one invalid state left. The last Section gives a summary of the whole paper.

II. BACKGROUND AND PREVIOUS WORK

A. Reversible Logic

According to Landauer's law, it is possible to achieve zero energy dissipation if operations are carried out in a reversible way. The reversible logic gate has a basic constraint: the number of inputs equals to that of output with one-to-one mapping. The inputs and the outputs can be recovered mutually, while fan-out and fan-in are not permitted in reversible circuits.

Toffoli has proved that the Toffoli gate is reversible, and it can achieve several basic logic functions like AND logic by changing the value of inputs. Bennett has demonstrated that the garbage bits generated during the computation could be removed by reversible operation in order to achieve physically reversibility[14]. As for the Toffoli gate, the reversible operation is the gate itself. If we cascade the gate twice, we can recover the input vectors at the output as shown below, which proves that the Toffoli gate is reversible in logic:

$$x \rightarrow x \rightarrow x$$

$$y \rightarrow y \rightarrow y$$

$$z \rightarrow [z \oplus (xy)] \rightarrow [z \oplus (xy)] \oplus (xy) \rightarrow z$$

B. Quantum gates

A reversible gate is made up of several primitive quantum gates. As the quantum operations are unitary, the nature of quantum mechanism is reversible. The number of basic quantum gates used to construct the reversible gate is the quantum cost which is used to evaluate the performance of a reversible circuit. The quantum gates can be divided into one-value gates, two-value gates, and multi-value gates. In particular, the one-value gates and two-value gates are realizable primitive quantum gates and their realization cost is one. Toffoli gate, Feynman gate, Fredkin gates and some other basic gates, composed of primitive quantum gates, are widely used to construct reversible circuits.

C. Previous Work

Many efforts have been done in reversible combinational circuits, but little attention is paid on reversible sequential circuits due to the problem of feedback until Toffoli demonstrates that the feedback doesn't violate the basic law of the reversible circuit[3]. In other words, the sequential circuits remain reversible as long as the transfer matrix is unitary[5].

Picton[6] firstly proposed the model of RS latch and RS flip-flop, but there exists a fan-out problem at the output of the model, which is not allowed in the reversible circuit. Rice modified the circuit based on Picton's model and proposed an improved model of RS latch[15].

After the basic reversible latch model was presented, a variety of flip-flop circuits were also proposed[16,17]. Rice constructed the RS flip-flop using reversible gates, the conventional logic gates are replaced with reversible gates directly. Thapliyal proposed a reversible master-slave D flip-flop using Fredkin gates and Feynman gates in his paper[18]. Besides, some other sequential application circuits based on the flip-flop, such as reversible counter, comparator and shift register, etc, have been proposed. Especially, the counter, which consists of multistage flip-flops and plays a vital role in the sequential logic circuit, has also been studied. Paper[19] proposes a 4-bit counter using reversible gates, paper[20] constructs a MOD-8 counter based on T flip-flop, and the detailed circuit is shown in Fig.1, with a classical circuit shown in Fig.2.

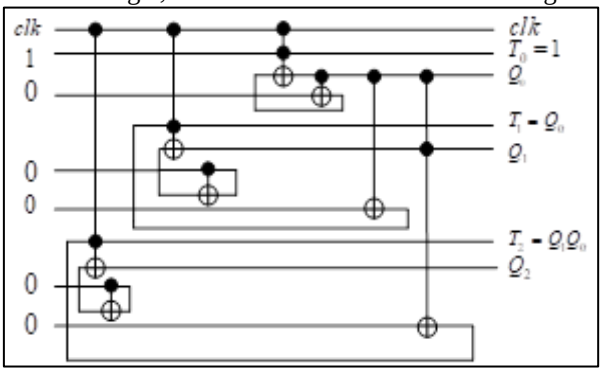

Fig. 1: reversible circuit of MOD-8 counter with TFF

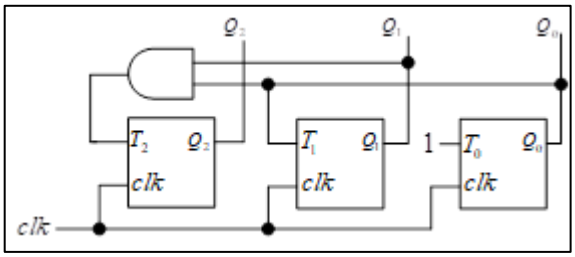

Fig. 2: classical circuit of MOD-8 counter with TFF

However, we have noticed that there exist some invalid states excluded from the count loop when we design the reversible counters. As a matter of fact, these invalid states greatly affect the counter, we have to consider the circumstance when the counter enters into the invalid states, which will cause the counter to fail. And what we expect is the counter can work properly even in the invalid states. Among existing papers, the reversible counter is designed and optimized in many ways but most of which are designed generally without considering the invalid states or just ignore the invalid states. Therefore, our paper focuses on the design of the self-start counter with invalid states, with special interest on that when the counter enters into the invalid states. Instead of replacing conventional logic gates directly, we present a novel method that keeps the reversible law by dividing the circuit into two parts to design self-start reversible counter, which will be introduced in the next section.

III. Design of Counter with Self-Starting

Many existing reversible designs can achieve a MOD-N counter composed of flip-flops, which satisfies the equation $N \leq 2^k$ (where k is the number of the flip-flop). If the number of states the counter achieves is less than 2^k, the counter will create one or more invalid states from which the counter cannot start counting, and it is one of the main reasons for the counter to enter failure mode. Hence, we design a reversible counter with the property of self-starting to resolve the problem of invalid states. This section mainly describes the design of reversible counter making full use of the invalid states and ensures the counter can start counting from any states including invalid states.

Regular reversible counter like MOD-8 or MOD-4 counter (with no redundant states) is designed via the truth table and state transition diagram where we can obtain the output expression in every flip-flop, and then construct the counter using reversible gates based on the expressions. Even though there exist invalid states like MOD-7 or MOD-6 counter, the reversible counter can still be constructed with that method, or in other words, the regular design of reversible counter does not consider the invalid states which do exist. Unlike the regular design of reversible counter, the self-start counter considers the invalid states, and especially focuses on how to deal with the irreversible problem that self-starting character brings during the design process, which makes self-start counter design significantly different from both the regular design of reversible counter and classical non-reversible self-start counter.

In order to let the invalid states be a part of the counting loop, we add the invalid states into the state transition diagram and reconstruct the truth table. In this

way, we can construct the reversible circuits theoretically. In our design, we combine the combinational circuit and sequential circuit to solve the irreversible problem emerging in design. The whole circuit can be divided into two parts. One is the regular design of the reversible counter, and the other is the self-starting part, but both of which are reversible. The sequential part achieves the basic function of regular counter, and the combinational part is used to judge whether the current state is invalid, with a single bit to control the next state. The design of the judgment circuit is mainly determined by the invalid states. At the input of the flip-flops, we used several Fredkin gates to make sure that the counter can enter the work mode from the invalid states under the control of the judgment circuit.

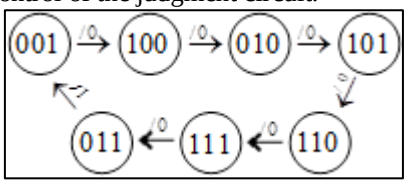

Fig. 3: (a) states transition diagram of MOD-7 counter

$Q_1^n Q_2^n Q_3^n$	$Q_1^{n+1} Q_2^{n+1} Q_3^{n+1}$
001	100
100	010
010	101
101	110
110	111
111	011
011	001

Fig. 3: (b) truth table of MOD-7 counter

Now we take a detailed illustration with an example of the MOD-7 counter composed of D flip-flop. According to the equation $N \le 2^k$ mentioned above, we found that it needs three D flip-flops to construct a MOD-7 counter. Fig.3 shows the state transition diagram and truth table of the MOD-7 counter. As we can see, there is a state '000' missing, which means that the counter can start counting directly from any states except the state '000', which is the invalid state. The output expressions at the output of D flip-flop can be readily obtained via the truth table in Eq.1

$$\begin{cases} Q_1^{n+1} = Q_2 \oplus Q_3 \\ Q_2^{n+1} = Q_1 \\ Q_3^{n+1} = Q_2 \end{cases} \quad (1)$$

We can obtain the regular design of a MOD-7 reversible counter based on the Eq. 1. But to ensure that the counter can count from any states including the invalid states, we add invalid states to the states transition diagram. In this design, we make the invalid state '000' point to the state '010' used as the next state in the loop so that the counter can enter into the work mode via the missing state as Fig.4 (a) shows. The truth table corresponding to the state transition diagram is shown in Fig.4 (b). We can get new expressions shown in Eq. 2 from the truth table of the self-start counter that differs from the regular design of the reversible counter:

$$\begin{cases} Q_1^{n+1} = Q_2 \oplus Q_3 \\ Q_2^{n+1} = Q_1 + \overline{Q_2}\,\overline{Q_3} \\ Q_3^{n+1} = Q_2 \end{cases} \quad (2)$$

But from the shaded part of the truth table shown in the Fig.4 (b), the problem is that the inputs and outputs are not mapping uniquely, which makes the basic condition of reversibility not satisfied. So we could not design the self-start counter with Eq. 2 obtained from the self-start truth table, which is different from the self-start counter in classical design. It is well known that the classical self-start counter is designed with Eq. 2.

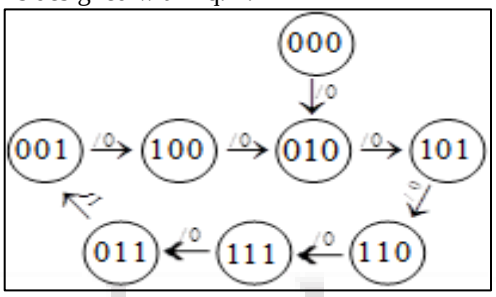

Fig. 4: (a) states transition diagram of MOD-7 counter

$Q_1^n Q_2^n Q_3^n$	$Q_1^{n+1} Q_2^{n+1} Q_3^{n+1}$
001	100
100	010
010	101
101	110
110	111
111	011
011	001
000	010

Fig. 4: (b) truth table of self-start counter

Considering both the irreversible problem and self-starting property, we divide the circuit into two parts, the main part of the circuit is still the regular reversible counter design based on the Eq. 1, and the rest of the circuit includes a judgment circuit and states transition circuit. We build the self-starting part using three Fredkin gates to achieve the transition of the invalid states. The complete circuit is shown in Fig.5.

We design a regular MOD-7 counter consisting of three D flip-flops based on the Eq.1 without considering invalid states. The self-starting part including judgment circuit and state transition circuits is realized separately to avoid the irreversible limitation. At the end of the last D flip-flop, a judgment circuit with Toffoli gates are used here

to determine whether the current state is invalid, and the last bit of judgment circuit is an enable bit T decided by the current state, the initial state of T is 0. There are three Fredkin gates used at the input of each flip-flop to implement states transition under the control of T. When T=0, the judgment circuit will not be active and the counter go on working normally. The missing state is '000', and the enable bit is decided by $T = Q_3 Q_2 Q_1$. As long as the invalid state '000' emerging, through the reversible judgment circuit, we will get the result $T = 1$ which controls three Fredkin gates to exchange the values of two inputs, and makes the next state '010'. Therefore the counter would be able to count from every state while satisfying the reversible condition simultaneously.

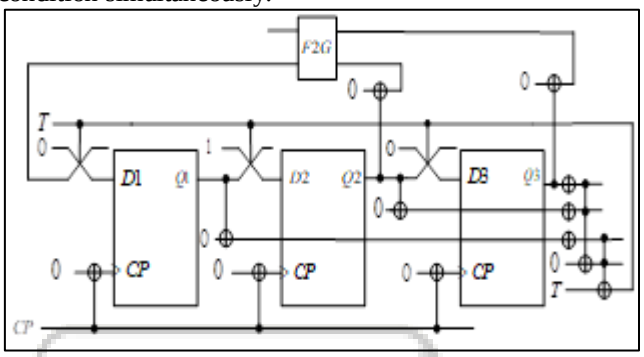

Fig. 5: the design of a MOD-7 self-start counter

IV. CONCLUSION

In this paper, we have proposed a novel design of counter using reversible gates with the property of self-starting. The proposed design resolves the invalid state effectively so that the counter can start counting from any states including the invalid states. We also present a new method to design a self-start reversible counter by combining the sequential and combinational circuit based on the truth table and state transition diagram to avoid the irreversible problem that self-starting property brings. It can be seen that the method differs greatly from the regular design of reversible counter and the classical self-start counter. This design can be used in the reversible counter including one or more invalid states, which can prevent the counter entering failure mode. Our work may provide an insight into the development of reversible circuits.

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