Voltage Controlled Oscillator for Digital Applications: A Review

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Abstract— Most signaling process systems need frequency or time reference signals. Oscillators are needed to get the carrying signals for radio wave transmission, however additionally for the most clocks of processors. This paper deals with the analysis and style of CMOS oscillator specifically voltage controlled oscillators (VCOs).Voltage Controlled signal generator is an electronic generator whose output frequency is controlled by a voltage input. VCO is designed with several circuit techniques. Primarily, there are ring oscillator, relaxation oscillator and resonant oscillator. There are various factors which should be considered which designing an oscillator i.e. stability, giant electrical tuning range, gain factor, linearity of frequency verses control voltage and cost. On the premise of that the comparison between CMOS VCOs is represented.

Key words: PLL, VCO

I. INTRODUCTION

Advancements of integration technologies and large scale system design made possible the electronics industry to achieve an outstanding growth over the last twenty years [1]. The large number of usage of integrated circuits in superior computing, telecommunications, and consumer electronics has been rising steadily, and at an awfully quick pace. Typically, the desired computational requirement (or, in alternative words, the intelligence) of those applications is leads to the quick development of this field [2].

The role of oscillators is to make a periodic digital or analog signal with a stable and sure frequency. Oscillators are needed to generate carrying signals for frequency transmission, however conjointly for the most clocks of processors. The voltage controlled generator (VCO) generates a clock with a governable frequency [3]. The VCO is often used for clock generation in phase lock loop circuits. The clock could vary generally by 50% of its central frequency.

VCO is that the primary phase within the several RF circuits and is the core of phase Lock Loop framework, Clock recovery circuit and Frequency Integrated circuits, thus it's exceptionally elementary to decide on the suitable VCO definition. Recurrence, adequacy need to be controlled for immense numbers of the applications.

A voltage-controlled oscillator (VCO) is used as the basic building block in basic and advanced circuits. As an example, a VCO is the elementary building block in phase locked loop (PLL) and clock generator circuits in present day microcircuits.

Within a phase locked loop (PLL), or frequency synthesizer, the performance of the voltage controlled oscillator (VCO) is of predominate importance. This is often as a result of the VCO Voltage Controlled Oscillator performance determines several of the performance characteristics of the synthesizer. In order that the PLL or synthesizer will meet its full specification a well-designed voltage controlled oscillator is important. Planning a extremely high performance voltage controlled generator-VCO, isn't invariably straightforward as there are many measure that require to be met. A careful design and a few experimentation a decent VCO design is possible.

These basic necessities for the VCO can govern several of the selections regarding the circuit topology and alternative basic aspects of the circuit. These fundamental necessities are:

A. VCO Tuning Range

It's obvious that the voltage controlled oscillator should be able to tune over the range that the loop is anticipated to control over. This demand isn't forever straightforward to satisfy and should need the VCO or resonator to be switched in some extreme circumstances.

B. VCO Tuning Gain

The gain of the voltage controlled oscillator is very important. It's measured in terms of volts per hurtz (or V/MHz, etc). As unit suggests it's the standardization shift for a given change in voltage. The voltage controlled oscillator gain affects a number of the general loop style concerns and calculations. The VCO response curve is seen to be comparatively straight at lower frequencies. But they unremarkably change form at higher voltages wherever the changes in capacitance from the varactor diodes cut back.

C. VCO V/f Slope

It's a key demand for any voltage controlled oscillator utilized in a PLL that the voltage to frequency curve is monotonic, i.e. it forever changes within the same sense, usually increasing frequency for increasing voltage. If it changes, as will happen in some instances unremarkably as a results of spurious resonances, etc, this may cause the loop to become unstable. Consequently, this should be prevented if PLL is to control satisfactorily. This curve shows atiny low dip and would end in the PLL turning into unstable.

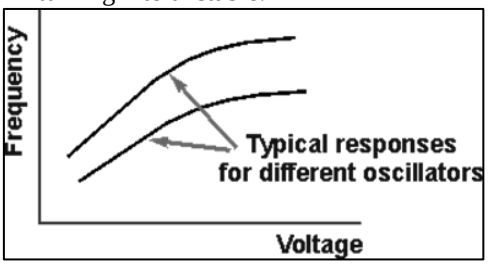


Fig. 1: Voltage Controlled Oscillator V/F Curves

Phase noise performance: The section noise performance of the voltage controlled generator is of specific importance in some PLL applications - notably wherever they're utilized in frequency synthesizers. Here the section noise performance of the VCO determines several of the general section noise performance characteristics of the general loop and therefore the overall synthesizer if utilized in one.

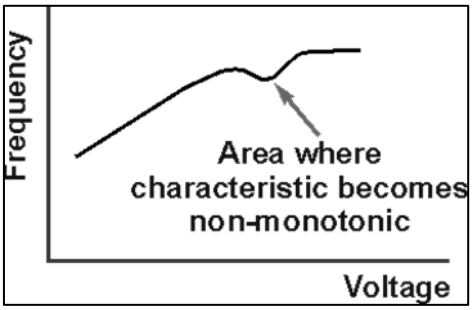


Fig. 2: Voltage Controlled Oscillator V/f Curves

II. VCO ARCHITECTURE

A VCO is considered as an amplifier and a feedback loop like an oscillator. The gain of the amplifier may be denoted as A & the feedback as B. Following architecture can be used to generate controlled oscillation:

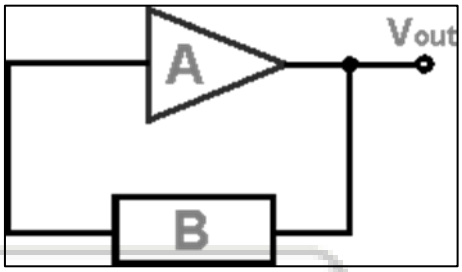


Fig. 3: Feedback around an Amplifier in an Oscillator

A. LC based VCO

In this form of design active devices, in addition to LC resonant circuits are used. High frequency oscillations. High frequency oscillations are generated using inductors and capacitors. Output will be an oscillating sinusoidal wave. This design is most popular wherever space and power aren't area of concern, as RL circuits may be large and a lot of power consumed.

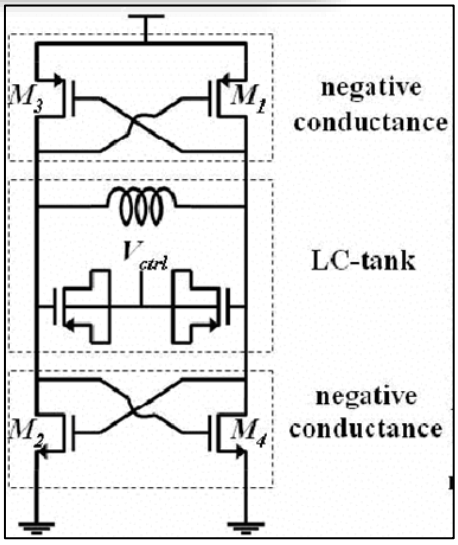


Fig. 4: Simple LC-VCO

A. Switched Capacitor based VCO

To increase the range of tuning of the VCO, a Switched capacitor Array technique has been used by many researchers. A CMOS VCO could comprise a primary inductance L_{p1} , a second inductance L_{p2}, two inversion mode NMOS variable capacitors, two n-channel metal oxide semiconductor (NMOS) transistors M1 and M2 and a bias current supply I. each the primary inductance L_{p1} and also the second inductance L_{p2} could also be derived from inductive effects of a sq. space from a wafer like a sq. spiral inductance. The pair of inversion NMOS variable capacitors are often enforced by two NMOS transistors. A lot of significantly, the drain terminals and also the supply terminals of the two NMOS transistors area unit tied along as a bearing terminal for fine-tuning the capacitance of the pair of inversion NMOS variable capacitors. By applying different control Voltages at the control terminal, the capacitance of the two inversion NMOS variable capacitors changes consequently. As a result, the oscillation frequency from the L-C tank made by the primary inductance L_{p1}, the second inductance L_{p2} and also the two inversion mode NMOS variable capacitors are often tuned over a range. As an example, once the control voltage varies from Zero volts to at least one volts, the oscillation frequency from the L-C tank are often tuned over 4GHz from 50 GHz to 54 GHZ. So as to more fine-tune the oscillation frequency of the L-C tank, an extra Switched capacitor array could also be connected with the pair of inversion mode NMOS variable capacitor in parallel. By switch on or off a capacitor bank of the Switched capacitor array, a fine standardization step of the L-C tank are often achieved. The switch transistors have an oversized dimension to enhance the Quality factor of the resonant tank circuit, ensuring improved phase noise performance.

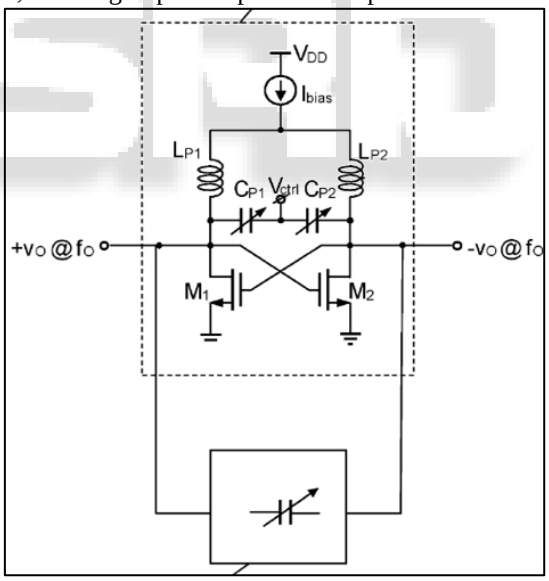


Fig. 5: A Cross Coupled Voltage Controlled Oscillator

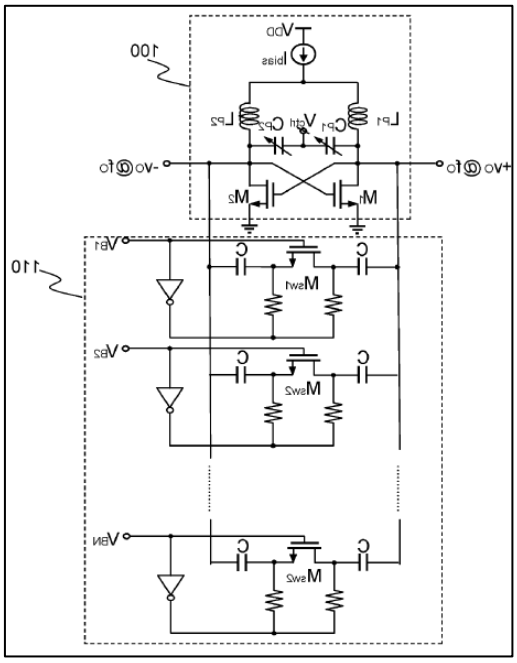


Fig. 6: an n-bit Switched Capacitor Array

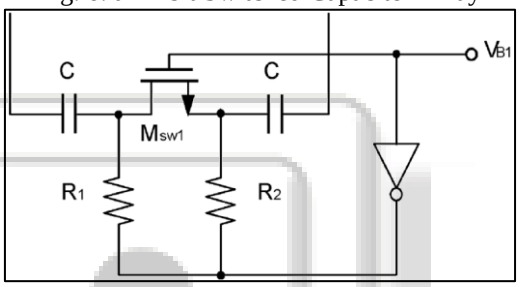


Fig. 7: a schematic diagram of a Capacitor Bank

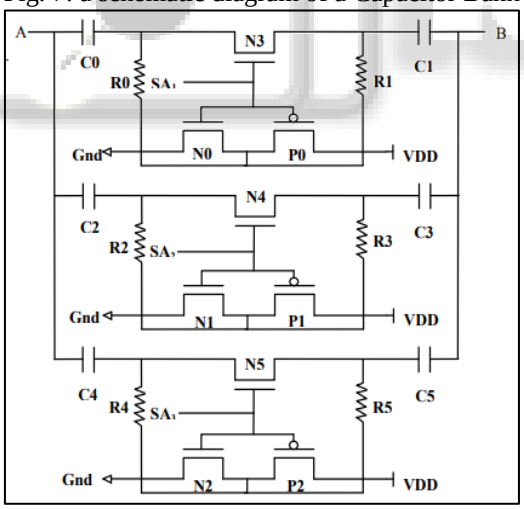


Fig. 8: a Schematic Diagram of a 3-bit Switched Capacitor Array

B. Ring Oscillator

In a CMOS ring generator, the output frequency will be controlled simply and conjointly on-chip inductors are not needed. A ring oscillator could be a closed-loop system circuit that consists of an odd variety of stages of identical inverters, forming an feedback oscillator. The feedback from the output of the last stage to its input causes the required oscillations. It desires solely an power supply to work and so oscillations begin thenceforth on its own. The frequency of oscillation will be more modified by either dynamic input voltage or dynamic number of stages.

The basic component in ring generator is an inverter. The inverter consists of complementary pairs of pmos and nmos. The 2 inverters are symmetric within the manner that parameters like channel length, doping are same for each the devices. Inverting operation means that once input is low output gets high and vice-versa[5]. The inverter is currently virtually employed in all digital styles. The behavior of any complicated circuit are often determined by estimating the results obtained for the inverters. All digital and analog circuits can be designed using this inverter circuit [6].

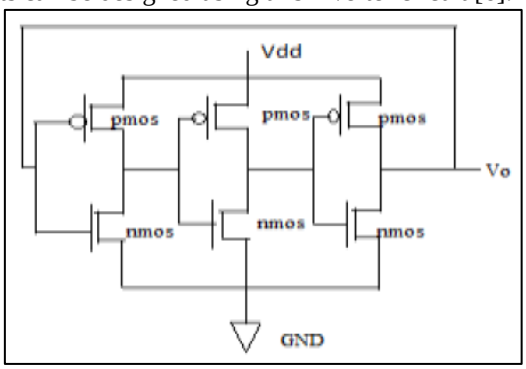


Fig. 9: A 3-Stage Ring Oscillator

In a ring generator, the gain stages are connected in a loop that output from the last stage is given to the input of initial stage. The circuit should satisfy the Barkhausen criteria so as to produce sustained oscillation, wherever the circuit ought to offer unity voltage gain and it should have a phase shift of 2π. The DC inversion provides π phase shift and also the remaining π phase shift is split equally among the stages in ring generator, therefore every delay provides phase delay of π/N, wherever N is variety of stages in an oscillator[8]. A basic three stage ring generator is shown in fig 9.

There are several measure that may decide the performance of any circuit. One of them is delay that's provided from one stage to a different. Here, every inverter gives a delay between the stages, referred to as propagation delay (φd). This propagation delay is that the average of high to low and low to high transition delay in every stage.

$$\varphi d = \varphi lh + \varphi hl$$

Second issue that decides performance of ring generator is its frequency. For N stage, generator frequency is given as:

$$f_{osc} = \frac{1}{\varphi d} = \frac{1}{2N\varphi}$$

Where $\varphi = \varphi lh = \varphi hl$ [9].

The frequency of the ring generator depends upon the φ that successively depends on the circuit parameters. the 2 parameters φlh and φhl may be determined for one stage ring oscillator from the equations given below:

$$\varphi hl = \frac{c}{gN(v_{dd} - v_{tn})}\left\{\frac{2v_{tn}}{v_{dd} - v_{tn}} + \ln\left(\frac{3v_{dd} - 4v_{tn}}{v_{dd}}\right)\right\}$$

$$\varphi lh = \frac{c}{gp(v_{dd} + v_{tn})}\left\{\frac{2v_{tp}}{v_{dd} + v_{tn}} + \ln\left(\frac{3v_{dd} + 4v_{tn}}{v_{dd}}\right)\right\}$$

Where gN and gP are transconductance, Vtn and Vtp are threshold voltages of nmos and pmos transistors respectively, v_{dd} is power offer and C is capacitive load[10]. Another issue that's of main concern is power consumption

of this circuit that depends on offer voltage. For economical operating of the device, the circuit ought to consume less power. N-stage ring oscillator consumes power p_{avg} given as :

$$p_{avg} = \eta\, v_{dd} * I_{avg} = \eta\, N\, v_{dd}\, Q_{max}\, f_{osc}$$

Where η is the efficiency of the given circuit and I_{avg} is the average current.

$$Q_{max} = C_{tot} * v_{dd}$$

And I_{avg} can be calculated as

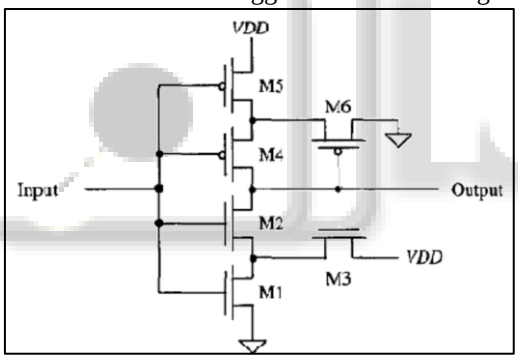
$$I_{avg} = N * C_{tot} * v_{dd} * f_{osc}$$

Where C_{tot} is the total capacitance.

When power supply is increased in the ring oscillator will leads to the increased frequency and power consumption and reduced delay.

C. VCO using Schmitt Triger

The Schmitt Trigger could be a comparator with 2 completely different threshold voltage levels. Whenever the input voltage goes over the High intensity level, the output of the comparator is switched high or low. The output can stay during this state, as long the input voltage is more than that of the second threshold level. Once the input voltage goes below this level, the output of the Schmitt Trigger can switch. The high and low output voltages are literally the positive and negative power provide voltages of the comparator. The comparator must have positive and negative power provide (like + and -) to control as a Schmitt Trigger. CMOS implementation of Schmitt trigger circuit is as in fig 10.



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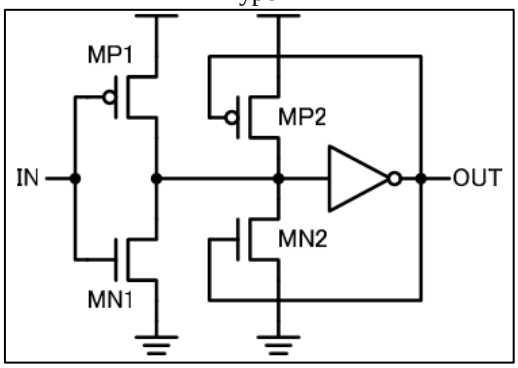


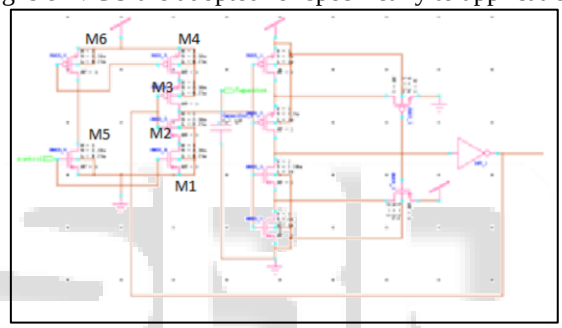
Type 2

Fig 10: CMOS Implementation of Schmitt Trigger

Voltage controlled Oscillator using the Schmitt trigger is shown in Fig.11. Here the MOSFETs MI and M4 behave as current sources mirroring the present in M5 and M6. once the output of the oscillator is low, M3 is on and M4 is off. this permits the constant current from M4 to charge C. once the voltage across C reaches Highest input voltage the output of the Schmitt trigger swings low. This causes the output of the oscillator to travel high and permits the constant current from M1 to discharge C. once C is discharged all the way down to Lowest input voltage the Schmitt trigger changes states. This series of events continues, generating the sq. wave output. Here the Schmitt trigger used will replaced by any CMOS enforced Schmitt trigger giving rise to different wave output depending on the schmitt trigger circuit.

III. CONCLUSION

Oscillators are elementary component of various electronic circuit designs. Voltage Controlled Oscillator can be used in various applications like Frequency Shift Keying, Frequency identifiers, Keypad Tone recognizers, Clock/Signal/Function Generators and used to build Phase Locked Loops. The voltage controlled oscillator is the main function block in a Phase Locked Loop system. This paper presents a study regarding voltage controlled oscillator, diagram of voltage controlled oscillator is shown and at last architecture of different voltage controlled oscillator are presented. The designs of VCO are adopted for specifically to applications.



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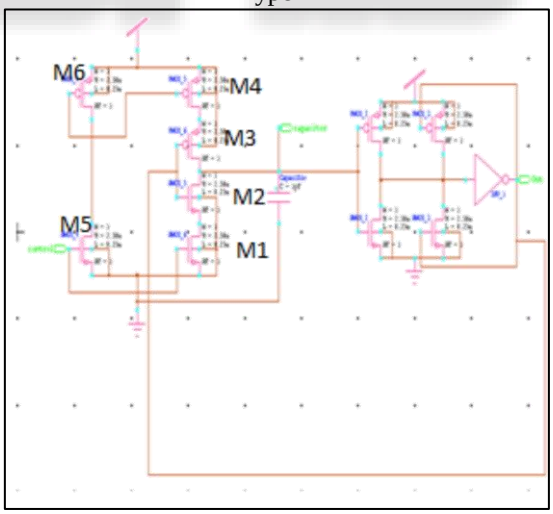

Type 2

Fig. 11: CMOS implementation of VCO Using Schmitt Trigger

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