

A Dual Compensation Control in Unified Power Quality Conditioner (UPQC) for Power Quality Improvement in Distribution System with Non-Linearity

Pappu Kumar¹ Preeti Gupta²

¹P.G. Scholar ²Assistant Professor

^{1,2}Department of Electrical & Electronics Engineering

^{1,2}Oriental College of Technology, Bhopal (M.P.), India

Abstract— In this research a dual compensating scheme based UPQC (Unified Power Quality Conditioner) controller has been designed for compensating source condition for all non-linear loading. The focus of the research is to mitigate harmonics in the supply system generated due to nonlinear loading and maintain the supply profile at all adverse conditions. UPQC is featured with dual compensation strategy such that it employs two converters. One is connected in series through a coupling transformer. Another is in parallel connected at load side. The controlled quantities are in synchronous frame. This simplifies the control algorithm of the topology. The performance of the system has been examined under various nonlinear loadings.

Key words: Multilevel inverter (MLI), Neutral Point Clamped (NPC), Flying Capacitor, Cascaded H-bridge, SPWMS, VMSHE-PWM, Sigma-delta Modulation

I. INTRODUCTION

There are two major sources which creates power quality issues at utility side one is increasing penetration of distributed generation and increase of nonlinear loading. DGs and nonlinear loading causes distortion of supply voltage. The root cause behind this is power electronic converters (PEC). PECs injects harmonics into the supply voltage and distorts the load as well as source currents. Other PQ (power quality) problems, such as voltage unbalances and voltage sags/swells can also affect the proper operation of sensitive equipment causing malfunction voltage sensitive equipments. PQ has been a sever threat for the stable operation of power system and a lot of research has been done and still a lot scope to mitigate PQ issues.

PECs are the root cause of PQ related problems and solution is also hidden in proper design and control mechanism of PECs to mitigate PQ related problems. When converters are properly designed and properly placed in the system they are the best solution for PQ problems.

Technically PECs which are used to mitigate PQ problem and improves the performance of the distribution systems are termed as custom power devices (CPD). The concept behind CPD is to add value to the power that is offered to the customer aiming to improve power quality and reliability.

In literature numerous CPDs are available such as; Active Power Filters (APF), Surge Arresters (SA). Battery Energy Storage

Systems (BESS), Super conducting Magnetic Energy Systems (SMES), Static Electronic Tap Changers (SETC), Solid State Fault Current Limiter (SSFCL), Solid-State Transfer Switches (SSTS), Static VAR Compensator (SVC), Distribution Series Capacitors (DSC), Dynamic Voltage Restorer (DVR), Distribution Static synchronous

Compensators (DSTATCOM) and Uninterruptible Power Supplies (UPS), Unified power quality conditioner (UPQC). Among these UPQC [1] – [17] is widely used which is designed using two APFs; shunt [18]–[24] and series [25]. Shunt APFs are placed in parallel with nonlinear loads, and controlled to operate as a sinusoidal current source. Series APF is connected between nonlinear load and the utility through a coupling transformer mitigating load harmonic currents. With the help series and parallel APFs UPQC is able to adopt dual compensating strategy that means it can perform both series and parallel power line conditioning simultaneously. The conventional UPQC is designed with nonsinusoidal reference frame which is very difficult to be synthesized by pulse width-modulated (PWM) converters and require an additional effort in order to achieve good performance. While sinusoidal reference frame (SRF) are easy to implement and has better performance.

In this research also series APF is controlled as sinusoidal current source with high impedance to block the load harmonic current to enter into the supply system and parallel converter is controlled as sinusoidal voltage source with low impedance to absorb the load harmonic currents. Hence the proposed topology is termed as dual compensating UPQC system. Thus, different from the conventional conditioning strategy, which uses nonsinusoidal control references, the dual compensating strategy uses only sinusoidal references to control the PWM converters. As a result, the generation of the control references is easier to obtain, allowing the use of simpler algorithms to accomplish this aim.

II. UNIFIED POWER QUALITY CONDITIONER

The best protection for sensitive loads from sources with inadequate quality is shunt- series connection i.e. unified power quality conditioner (UPQC). Recent research efforts have been made towards utilizing unified power quality conditioner (UPQC) to solve almost all power quality problems for example voltage sag, voltage swell, voltage outage and over correction of power factor and unacceptable levels of harmonics in the current and voltage. The basic configuration of UPQC is shown in figure 1

The main purpose of a UPQC is to compensate for supply voltage flicker/imbalance, reactive power, negative-sequence current, and harmonics [14]. In other words, the UPQC has the capability of improving power quality at the point of installation on power distribution systems or industrial power systems. The UPQC, therefore, is expected as one of the most powerful solutions to large capacity sensitive loads to voltage flicker/imbalance.

Unified Power Quality Conditioner (UPQC) for non-linear and a voltage sensitive load has following facilities:

It eliminates the harmonics in the supply current, thus improves utility current quality for nonlinear loads. UPQC provides the VAR requirement of the load, so that the supply voltage and current are always in phase, therefore, no additional power factor correction equipment is necessary.

UPQC maintains load end voltage at the rated value even in the presence of supply voltage sag.

The voltage injected by UPQC to maintain the load end voltage at the desired value is taken from the same dc link, thus no additional dc link voltage support is required for the series compensator.

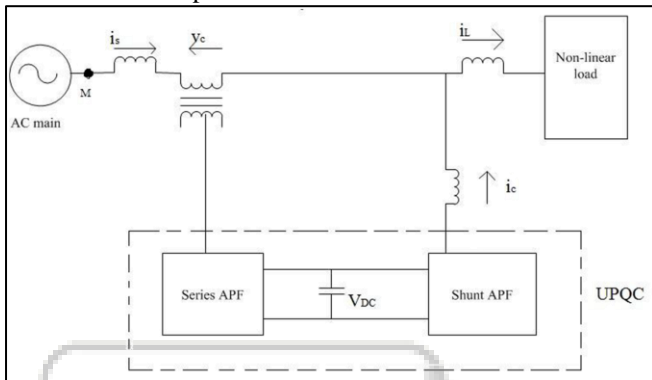


Fig. 1: Schematic of UPQC

III. CONTROL OF UPQC

Conventionally UPQC are controlled nonsinusoidally. It is difficult to develop control algorithm for APF which are nonsinusoidal. Additional control is desired to improve the performance of such system. In this work UPQC are controlled sinusoidally hence less effort is required to control shunt and series APF. Such type of control is called synchronous reference frame (SRF). SRF control resembles the instantaneous control theory. The characteristics property of this strategy is that only load current is essential here for the generation of reference current and hence disturbances present in source or distortions present in voltage have will leave no negative impact on the performance of the designed UPQC system. In the proposed topology, the three phase voltage or current signals are sensed and to develop the control signal they are transformed from abc to rotating dq0 frame using parks transformation. The transformation angle (ωt) is angular position of proposed reference frame. This ωt is rotating at constant speed and is synchronized with the 3- ϕ ac voltage using PLL. After this, currents having same magnitude but with reverse phase is produced and injected to the proposed system for compensating neutral current, harmonics, and reactive power. In the stationary reference frame abc coordinates are stationary, while in the SRF, d-q-0 coordinate is rotating in synchronism with supply voltages. This is presented in Figure 2.

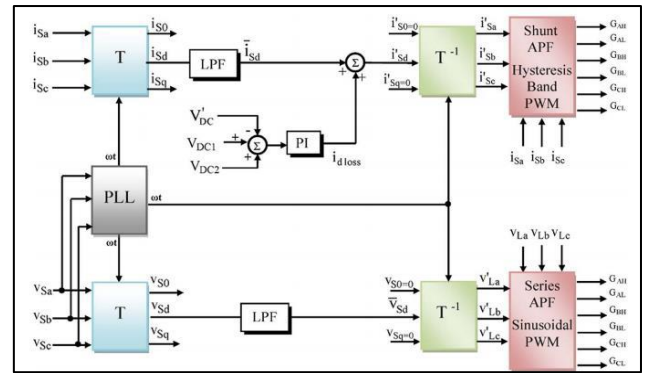


Fig. 2: SRF control for UPQC operation

From figure 2 it is clear that two controls are developed; one for series APF and another for shunt APF. The series APF acts as a controlled sinusoidal current source whose three phasecurrent is transformed into dq0 using park's transformation as in equation (1)

$$\begin{bmatrix} I_{so} \\ I_{sd} \\ I_{sq} \end{bmatrix} = T \begin{bmatrix} I_{sa} \\ I_{sb} \\ I_{sc} \end{bmatrix} \quad (1)$$

Where,

$$T = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} \sin(\omega t) & \cos(\omega t) \\ \frac{1}{\sqrt{2}} \sin(\omega t - 120^\circ) & \cos(\omega t - 120^\circ) \\ \frac{1}{\sqrt{2}} \sin(\omega t + 120^\circ) & \cos(\omega t + 120^\circ) \end{bmatrix} \quad (2)$$

The reference current is again obtained from inverse park's transform.

The shunt APF acts as a sinusoidal voltage source. The supply voltage is sensed and then it is transformed into d-q-0 frame of reference by the following transformation matrix:-

$$\begin{bmatrix} V_{so} \\ V_{sd} \\ V_{sq} \end{bmatrix} = T \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \quad (3)$$

Both the measured and reference source current are compared now and are synthesized using PI controller for getting the gating signals for operation of shunt and series APF in the given UPQC model and thereby eliminating all the current related problem from the system.

IV. SIMULATION

The scope of the research is to improve the power quality under various loading condition and voltage sag or transients. In this research a dual compensating scheme based UPQC (Unified Power Quality Conditioner) controller has been designed for compensating source condition for all non-linear loading.

Three types of loading has been tested in the proposed work through three phase and single phase rectifier as shown in Table 1. The designed system performance is also tested for the condition of voltage sag and the results are presented in this section.

Unbalanced three phase loads

Three single phase rectifier with RL loading
 Phase A Phase B Phase C
 R=8.1 ohm R=10.12 ohm R=8.1 ohm
 L=380mH L=346mH L=357mH

Three single phase rectifier with RLC loading
 Phase A Phase B Phase C
 R=13.5 ohm R=10.12 ohm R=8.1 ohm
 C=940 microFL=346mH L=380mH

Balanced loading connected via three phase full wave rectifier R=17 ohm

Table 1 Three types of loading

The focus of the research is to mitigate harmonics in the supply system generated due to nonlinear loading and maintain the supply profile at all adverse conditions. The schematic presentation of the proposed topology is shown in figure 3. Table 2 presents the design parameter of the system.

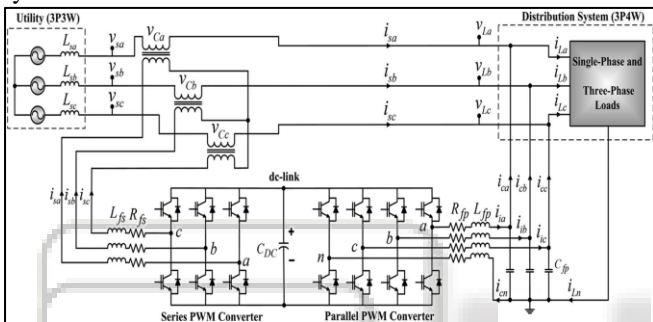


Fig. 3: distribution system connected with the proposed UPQC topology

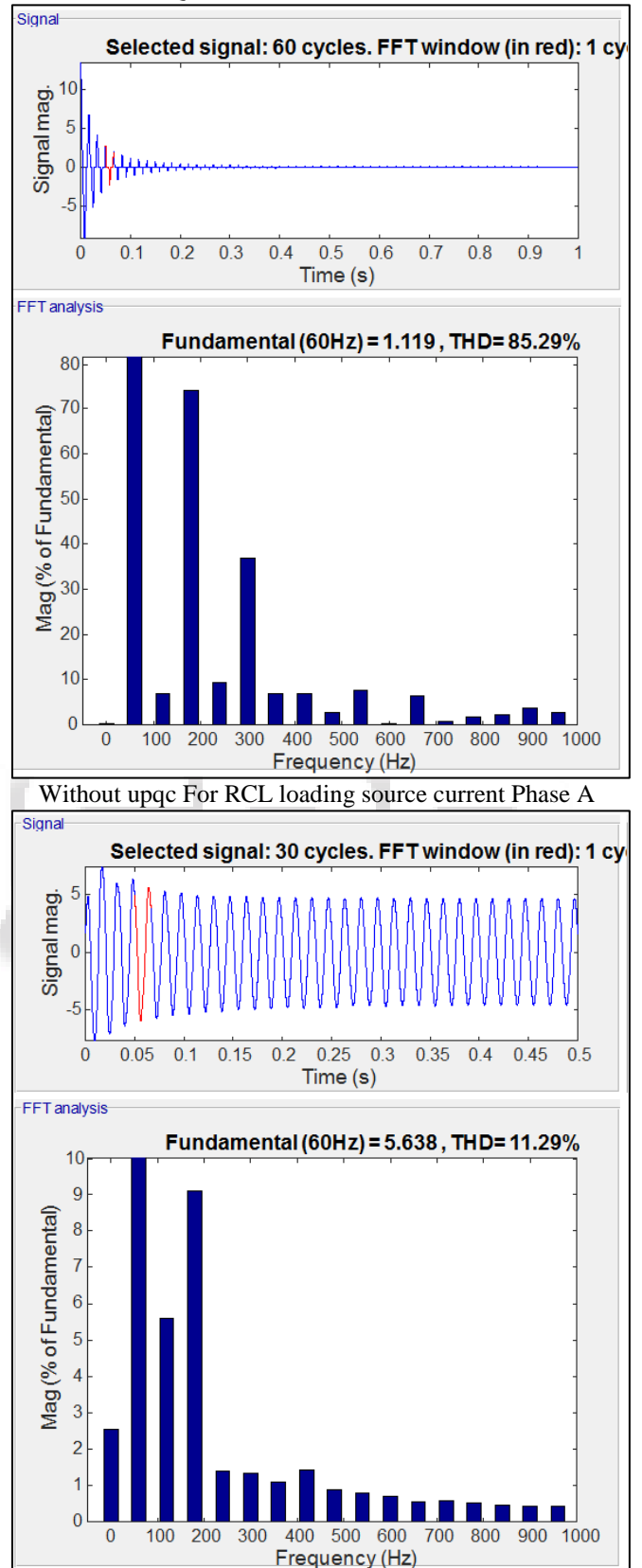
Effective nominal voltage of the utility (line to neutral)	Vs a , b , c = 127 V
Nominal utility grid frequency	fs = 60 Hz
Series filter inductance and capacitance	11H, 28e-6H
Inductance, resistance and Capacitances of the parallel	13e-6H, 10 ohm, 50e-6F
Transformation ratio of the series coupling transformers	n = 1
dc-bus voltage	Vd c = 400 V
dc-bus capacitance	Cd c = 9400 μF

Table 2: design parameters

V. RESULT & DISCUSSION

The performance of the system has been studied in three types of nonlinear loadings; three phase unbalanced RL and RC load connected via three single phase rectifier and balanced three phase resistive load connected through three phase rectifier. Also proposed system has been analyzed for the condition of voltage sag and transients. The system is analyzed with and without UPQC connected. The results are compared for THD percentage both source current and load current and it is found that source side THD are reduced more than 50% and even 100% in some cases. This means proposed UPQC topology is capable in preventing the propagation of harmonic currents source side. The results for the comparative analysis of with and without UPQC distribution system is shown in Table 3 and 4. Figure 4

presents the comparison of source current for phase A with and without UPQC.



With UPQC for RCL loading source current Phase A
 Fig. 4: comparison of THD for fundamental waveform of source current for RCL loading

Loading condition	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
	Without UPQC			With UPQC		
Three single-phase full-wave rectifiers (unbalanced load 1)	41	45	53	11.3	12	14.7

Three single-phase full-wave rectifiers (unbalanced load 1)	37.3	45	55	6.4	13.7	11.7
Balanced three-phase load Three phase full-wave Rectifier	27	27	27	1	1	1

Table 3: Comparison of Source Current THD with and without UPQC

Loading condition	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
	Without UPQC			With UPQC		
Three single-phase full-wave rectifiers (unbalanced load 1)	41	45	53	21	22	25
Three single-phase full-wave rectifiers (unbalanced load 1)	41	42	44	54	24	23
Balanced three-phase load Three phase full-wave Rectifier	27.5	27.7	27.6	16	16	16

Table 4: Comparison of Load Current THD with and without UPQC

VI. VOLTAGE SAGS (DIPS)

Voltage sag had been introduced at distribution side and the results are compared for with and without UPQC in this section. Figure 5 presents the performance of UPQC under voltage sag disturbance (Voltage phase “a”): Load side. The THD is very negligible that is 0.38%. Figure 6 shows the THD of the system connected with UPQC under voltage sag disturbance (Voltage phase “a”): Source side. And it can be seen that THD is almost zero. In figure 7 the fundamental waveform and THD analysis for load current is presented.

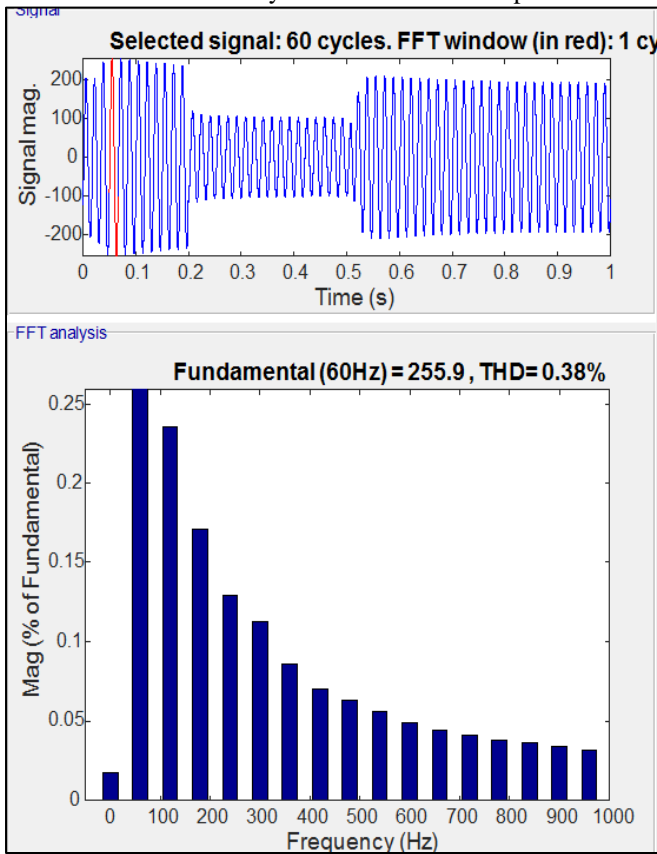


Fig. 5: UPQC under voltage sag disturbance (Voltage phase “a”): Load side

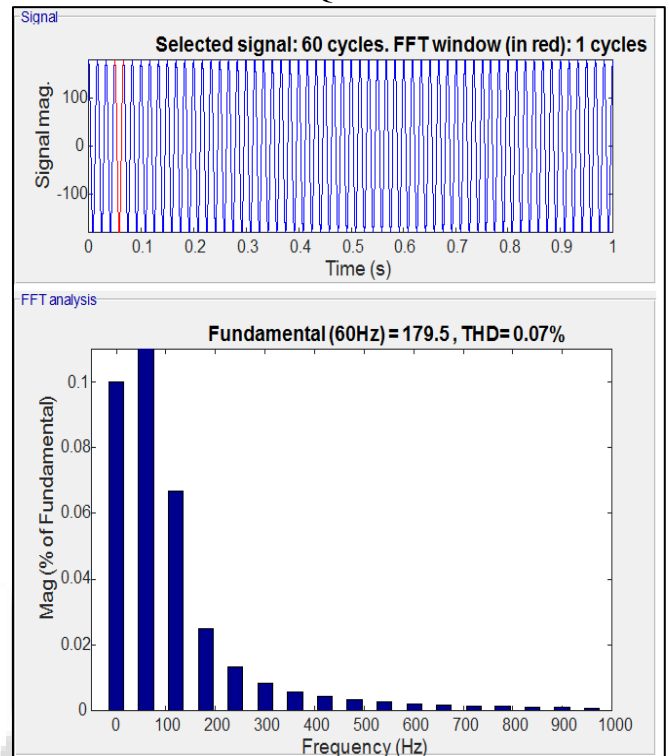


Fig. 6: UPQC under voltage sag disturbance (Voltage phase “a”): Source side

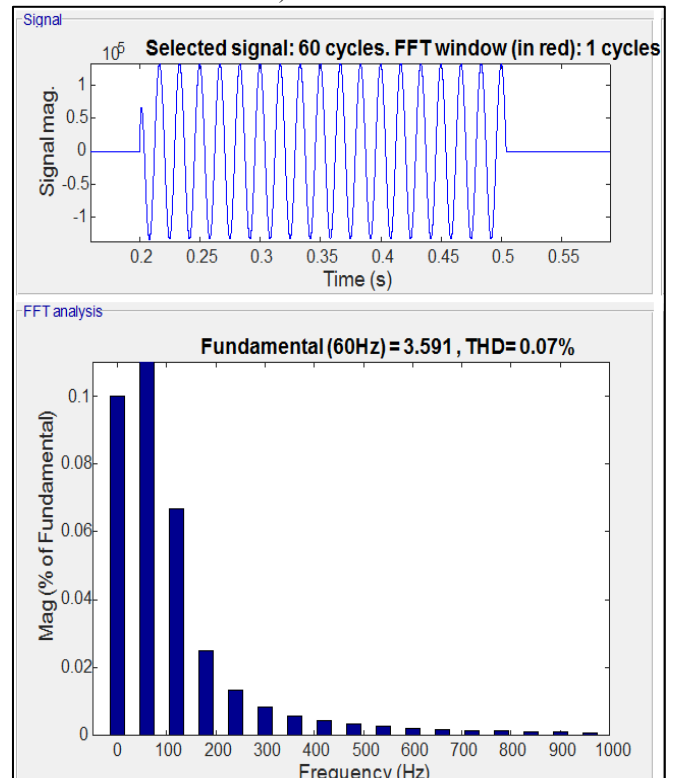


Fig. 7: System with UPQC under voltage sag load current

VII. CONCLUSION

This work presents the practical implementation of UPQC system connected to the three phase distribution system to eliminate the load current as well source harmonics.

With the help of series and parallel active filters input and output currents are balanced, and regulated. The system has been analysed under various nonlinear loading condition. Also the behavior of the proposed UPQC custom power device is studied under the condition of voltage dip.

The proposed topology is performing satisfactorily under various operating condition and mitigates the load as well as source harmonics.

REFERENCES

- [1] Rodriguez, et al, "Multilevel converters: An enabling technology for high-power applications," in Proc. the IEEE, vol. 97, no. 11, November 2009, pp. 1786-1817.
- [2] I. Colak, E. Kabalci, and R. Bayindir, "Review of multilevel voltage source inverter topologies and control schemes," Energy Conversion and Management, vol. 52, no. 2, pp. 1114-1128, February 2011.
- [3] P. K. Dewangan and U .T. Nagdeve, "Review of an inverter for grid connected Photovoltaic (PV) Generation System". International Journal of Scientific & Technology Research, vol. 3, no. 10, October 2014.
- [4] I. D. Pharne and Y. N. Bhosale, "A review on multilevel inverter topology," in Proc. International Conference on Power, Energy and Control, 2013, pp. 700-703.
- [5] S. S. Das, S. C. Gupta, and U. Rajkiran, "Harmonic mitigation in wind energy conversion system by multilevel inverter," International Journal of Electrical, Electronics and Data Communication, vol. 2, no. 9, September, 2014.
- [6] R. Seyezhai and B. L. Mathur, "Hybrid multilevel inverter using ISPWM technique for fuel cell applications," International Journal of Computer Applications (0975 - 8887), vol. 9, no.1, pp. 41-46, November 2010.
- [7] Leopoldo, et al, "The age of multilevel inverter arrives," IEEE Industrial Electronics Magazine, pp.28-39, June 2008.
- [8] S. Cherukuru, C. Joel., S. J. Jonish, and K. Sathiyasekar, "New modified cascaded H-bridge multilevel inverter topology with reduced switches," International Journal of Engineering Trends and Technology, vol. 9, no. 4, pp. 178-181, March 2014.
- [9] I. Vinodkumar and S. Hariprasad, "Modeling of new multilevel inverter topology with reduced number of power electronic components," in Proc. International Conference on Innovations in Electrical & Electronics Engineering, Hyderabad, 2014, pp. 23-30.
- [10] S. Divya and G. Umamaheswari, "Voltage unbalance elimination in multilevel inverter using coupled inductor and feedback control," International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, vol. 3, no. 4, pp. 9253-9258, April 2014.
- [11] I. Rajashekar, T. P. Kumar, Cascaded H-bridge multilevel inverter with a new selective harmonic mitigation technique to meet grid codes under non-equal Dc link voltages with power quality enhancement," International Journal of Innovative Research in Science, Engineering and Technology, vol. 3, no. 9, pp. 15857-15863, September 2014.
- [12] A. Tuteja, A. Mahor, and A. Sirsat, "A review on mitigation of harmonics in cascaded H-bridge multilevel inverter using optimization techniques," International Journal of Emerging Technology and Advanced Engineering, vol. 4, no. 2, pp. 861-865, February 2014.
- [13] H. Sira-Ramírez and R. Silva-Ortigoza, Control Design Techniques in Power Electronics Devices, 1st ed. Mexico City, ch. 6, pp. 361-366.
- [14] K. B. Bhaskar1, T. S. Sivakumaran, and M. Devi, "Implementation of 11 level cascaded multilevel inverter using level shifting pulse width modulation technique with different loads," IPASJ International Journal of Electrical Engineering, vol. 2, no. 10, pp. 20-31.
- [15] P. Premananth and S. B Chitrapreyanka, "A new multilevel inverter topology for DC-AC conversion," International Journal of Innovative Research in Science, Engineering and Technology, vol. 3, no. 2, pp. 194-202.
- [16] P. Sanjeevikumar, "Analysis and implementation of multiphase-multilevel inverter for open-winding loads," Ph.D. dissertation, Dept. Elect. Eng., Univ. Of Bologna, Bologna, Italy, March 2012.
- [17] L. M. Tolbert and F. Z. Peng, "Multilevel converters as a utility interface for renewable energy systems," IEEE Power Engineering Society Summer Meeting, vol. 2, pp. 1271-1274, July 2000.
- [18] W. A. Hill and C. D. Harbourt, "Performance of medium voltage multilevel converters," in Proc. 34th IAS Annual Meeting IEEE Industry Application Conference, vol. 2, Oct. 1999, pp. 1186-1192.
- [19] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: Survey of topologies, controls, and applications," IEEE Transactions on Industry Applications, vol. 49, no. 4, pp. 724-738, Aug. 2002.
- [20] S. Khomfoi and L. M. Tolbert, Multilevel Power Converters, Chapter 17, Power Electronics Handbook, 2nd Ed., Elsevier, 2007.
- [21] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," IEEE Power Electronics Specialists Conference, PESC'92, vol. 1, pp. 397-403, 1992.
- [22] J. S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," IEEE Transaction on Industry Application, vol. 32, no. 3, pp. 509-517, May/June 1996.
- [23] I. H. Shannon, Multilevel Converters: The Future of Renewable Energy: Design, Simulation and Implementation of a Multilevel Converter, pp. 05-43, LAP LAMBERT Academic Publishing USA, November 6, 2012.
- [24] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," IEEE Transactions on Industry Applications, vol. 35, no. 1, pp. 36-44, 1999.
- [25] S. Daher, Analysis, Design and Implementation of a High Efficiency Multilevel Converter for Renewable

- Energy System, PhD Dissertation, and University press GmbH kessel, 2006.
- [26] S. Khomfoi and L. M. Tolbert, *Multilevel Power Converters*, ch. 17, *Power Electronics Handbook*, 2nd Edition, Elsevier, 2007.
- [27] F. Z. Peng, "A generalized multilevel converter topology with self-voltage balancing," *IEEE Transactions on Industry Applications*, vol. 37, no.2, pp. 611–618, Mar./Apr. 2001.
- [28] W. A. Hill and C. D. Harbourt, "Performance of medium voltage multilevel converters," in *Proc. 34th IAS Annual Meeting IEEE Industry Application Conference*, vol. 2, Oct. 1999, pp. 1186–1192.
- [29] A. V. Zyl, J. H. R. Enslin, and R. Spee, "A new unified approach to power quality management," *IEEE Transactions on Power Electronics*, vol. 11, no. 5, pp. 691-697, Sept. 1996.
- [30] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A survey on cascaded multilevel inverters," *IEEE Trans on Industrial Electronics*, vol. 57, no. 7, pp. 2197-2206, July 2010.
- [31] N. Mittal, B. Singh, S. P Singh, R. Dixit, and D. Kumar, "Multilevel inverters: Survey of topologies, controls, and applications," in *Proc. 2nd International Conference on Power, Control and Embedded System*, 2012, pp. 978-986.
- [32] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: Survey of topologies, controls, and applications," *IEEE Transactions on Industry Applications*, vol. 49, no. 4, pp. 724-738, Aug. 2002.
- [33] P. W. Hammond, "A new approach to enhance power quality for medium voltage AC drives," *IEEE Transaction on Industry Applications*, vol. 33, no.1, pp. 202–208, Jan./Feb. 1997.
- [34] I. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Transaction on Industrial. Electronics*, vol. 49, no.4, pp. 858-886, 2002.
- [35] Z. Du, L. M. Tolbert, and J. N. Chiasson, "Active harmonic elimination for multilevel converters," *IEEE Transaction on Power Electronics*, vol. 21, no. 2, pp. 459-469, March 2006.
- [36] F. L. Lou, "Investigation on best switching angles to obtain lowest THD for multilevel DC/AC inverter," in *Proc. IEEE 8th Conference on Industrial Electronics and Application*, Anhui University, Hefei, China, 2013, pp. 1814-1818.
- [37] G. Shehu, T. Yalcinoz, and A. Kunya, "Modelling and simulation of cascaded H-bridge multilevel single source inverter using PSIM," in *Proc. World Academy of Science, Engineering and Technology, International Science Index 89, International Journal of Electrical, Robotics, Electronics and Communications Engineering*, vol. 8, no. 5, pp. 744 – 749, 2014.