Designing and Implementation of 9 Level Multi-Level Inverter with IPD Topology

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Abstract— The multi-level inverter system is very promising in ac drives, when both reduced harmonic contents and high power are required. A multilevel inverter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltages as inputs. Recently, multilevel power conversion technology has been developing the area of power electronics very quickly with good potential for further developments. As a result, the mainly attractive applications of this technology are in the medium to high voltage ranges. Multi-Level Inverters (MLI) are today used in medium and great power applications. There are three major topologies of multi level inverters; they are capacitor clamped, diode camped and cascaded. Throughout this research work implement the nine-level asymmetric cascaded multi level inverter with IM for various kinds of level-shifted PWM techniques in Matlab Simulink. As the number of levels will augment, the synthesized output waveform has more steps that produce a staircase wave that approaches the required waveform. Also, as more steps are added to the waveform, the harmonic distortion of the output wave decreases, similar to zero as the number of levels will increase. As the number of levels will increase, the voltage that can be spanned near between devices serial also increases.

Key words: MLI, EMC, PWM, IPD, APOD

I. INTRODUCTION

Inverters play vital role in routine life. In each field wherever electricity is needed inverters are going to be used there. The main function of the inverter is to convert DC input voltage to an AC output voltage of the specified magnitude. The output voltage waveforms of the ideal inverters ought to be sinusoidal however the wave style of the sensible inverters device is non-sinusoidal and contains fully completely different harmonics. Interest in multilevel power Inverters has been increased in the last decades when such kind of topologies were selected as the power Inverters of choice in many high voltage and high power applications, due to advantages of high quality waveforms low switch losses, high voltage capability and low electromagnetic compatibility (EMC) concerns. For low and medium power application square wave and quasi square wave voltage may be acceptable, and for high power purpose, low imprecise sinusoidal wave kind are needed with the arability of high speed power semiconductor devices designed with series affiliation of switch power devices. Harmonic content of output voltage can be decreased considerably by switching methods. The general idea of multilevel Inverters is to synthesize a sinusoidal voltage from several voltages of levels, typically obtained from capacitor voltage sources. As the number of voltage levels increases, the synthesized output waveform add more steps, producing a staircase wave which approaches the sinusoidal wave with minimum harmonic distortion The idea of multi-level inverter (MLI) was made since 1975, the multi-level long-term inverter (MLI) began with a three-tier structure. Multilevel inverter not only focused on medium and high power converter, but also allows the use of renewable energy sources. Multilevel topology inverter gives many advantages over two topology inverter level are: switching frequency may be reduced for the same switching losses and higher current harmonics output is reduced by the same switching frequency the voltage across switches is only half of the DC voltage. The general idea of the multilevel inverter (MLI) is obtained a voltage wave form near sine wave from several number of dc voltage levels, obtained from capacitor voltage source, as the number of level increase the synthesized output wave has more steps which produce a staircase wave that approaches desired output waveform also decreases the harmonic distortion of the output waveform

II. RESEARCH APPROACH

A multilevel converter device has many benefits over a standard two level converter device that uses high switching frequency pulse width modulation (PWM).

The enticing features of a multilevel converter device will be in brief as follows:

- They are suitable for high- voltage and high power current application. By using power device of lower voltage rating. Increased no. of levels which leads to better voltage waveform and reduce total harmonic distortion in output voltage.
- Reduced switching stresses due to the reduction of step voltage between the level
- It reduces the dv/dt stress, therefore electromagnetic capability (EMC) drawback will be reduced.
- No EMI drawback exists, as a result of they'll additionally increase equivalent switching frequency while not increasing of actual switch frequency therefore reducing ripple element of electrical converter inverter output voltage and electromagnetic interference.
- THD content decreased no of level increase and filtering requirement are reduced.
- Lower switching frequency means lower switching losses and higher efficiency.

Multilevel converters do have some disadvantages. One explicit disadvantage is that the bigger range of power semiconductor switches required. Though lower voltage rated switches will be utilized in an exceedingly construction device, every switch needs a connected gate drive circuit. This could cause the general system to be costlier and sophisticated. Modulation techniques and control paradigms have been developed for multilevel converters such as multicarrier pulse width modulation (MCPWM), sinusoidal pulse width modulation, selective harmonic elimination, space vector modulation, and others. In this thesis multicarrier pulse width modulation (MCPWM) is used.

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III. PROPOSED SYSTEM

The nine levels Asymmetric Cascaded multilevel inverter with three DC sources are used having three dissimilar and 12 power switches are used. The Asymmetric Multilevel Inverter increases the number of levels in the output and diminish the number of input DC sources necessitate. IGBT is used as semiconductor switch for scheming the inverter circuit. It has the high power rating, low conduction loss and low switching loss. This topology uses level-shifted multi carrier based original PWM method, use to construct a 9-level output voltage.

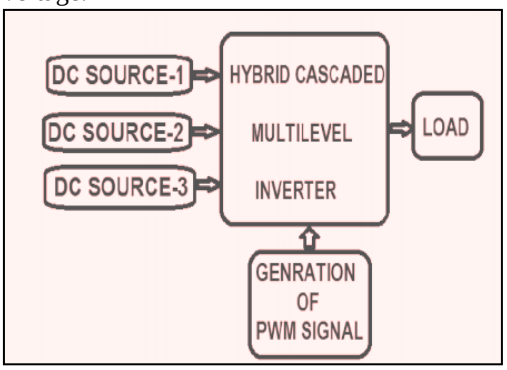

Fig. 1: Proposed Architecture of 9-levels Hybrid Cascaded Multilevel Inverter

IV. WORKING AND ANALYSIS

Working of this inverter is nothing but how we make power switches (IGBTs) ON and OFF as per voltage level desired. We have generated switching pulses to obtain staircase output voltage which resemble nearly equal to sine wave. For dissimilar switching angles the power circuit behaves another way producing different waveforms. In this topology, we have produced 9 voltage levels as 0, 100V, 200V, 300V and 400V.

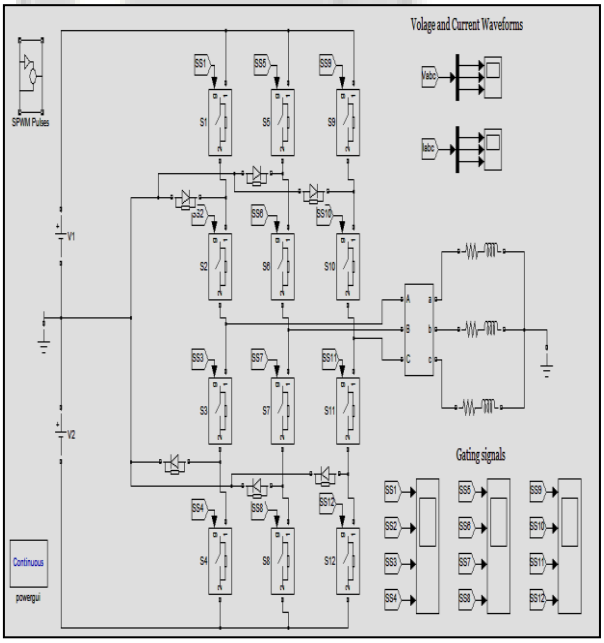

Fig. 2: Simulink model of 9 level with IM

A. *Switching Scheme*

A switching procedure was developed so that the topology can be modulated by the offset measurement pulse width modulation (PWM). These modulation systems can be applied to cascaded inverters H-bridge (CHB). A CHB inverter level m by using a multicarrier modulation scheme needs level shifted (m-1) of the triangular supports all having a frequency and amplitude similar. (M-1) of the triangular supports are arranged vertically the specified bands they occupy are contiguous. There are 3 different PWM methods with phase relationships for multicarrier modulations are developed staggered levels shown in Figure 3 and 4) In-phase disposition (IPD), where all carrier waveforms are in phase. 2) Phase opposition disposition (POD), where all carrier waveforms higher than zero reference are in phase but in opposition with those below the zero reference. 3) Alternative phase opposite disposition (APOD), where all carriers are alternatively in opposite disposition

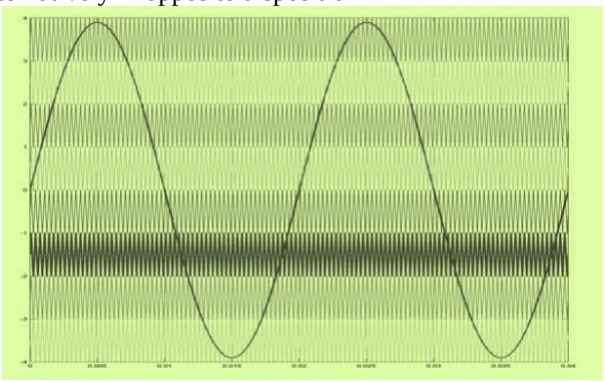

Fig. 3: Reference and carrier waveform for POD CLSPWM

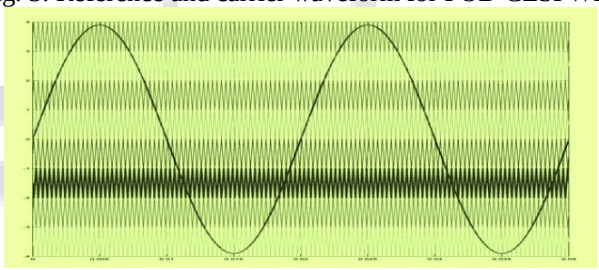

Fig. 4: Reference and carrier waveform for APOD CLSPWM

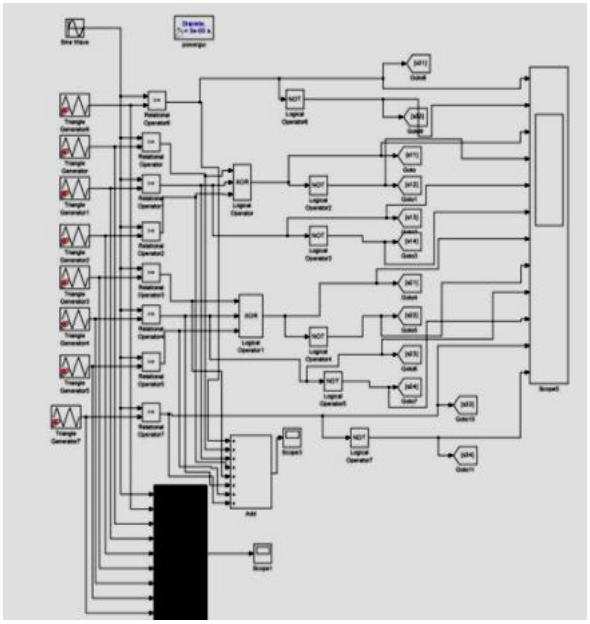

Fig. 5: Simulation model of control circuit of asymmetrical 9-level inverter

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Output	400V	300V	200V	100V	0V	-100V	-200V	-300V	-400V
S_1	1	1	1	1	1	0	0	0	0
S_2	1	1	0	1	0	0	1	0	0
S_3	0	0	0	0	1	1	0	1	1
S_4	0	0	1	0	0	1	1	1	1
S_5	1	1	1	0	0	0	0	0	0
S_6	1	1	1	1	0	1	0	0	0
S_7	0	0	0	0	0	0	1	1	1
S_8	0	0	0	1	0	1	1	1	1
S_9	1	0	0	0	0	0	0	0	0
S_{10}	1	1	1	1	0	1	1	1	0
S_{11}	0	0	0	0	0	0	0	0	1
S_{12}	0	1	1	1	0	1	1	1	1

Table 1: Switching pattern for asymmetrical cascaded nine level inverter

B. Simulation and Result

This chapter shows the comparative study of output voltage of 9-level asymmetrical cascaded multilevel inverters cascaded is compared for the PD, POD, APOD techniques ,and it also shows the THD profile and performance of the circuit with IM for three PWM techniques, and also the compare all result with 7-level MLI. Cascaded multi-level inverter shows the lowest THD profile without any type of filter and also any type of dependency of inductor and capacitor used for smooth the current wave form and due to less number of switching devices gate firing circuit also reduced that's why total cost and performance has been increased

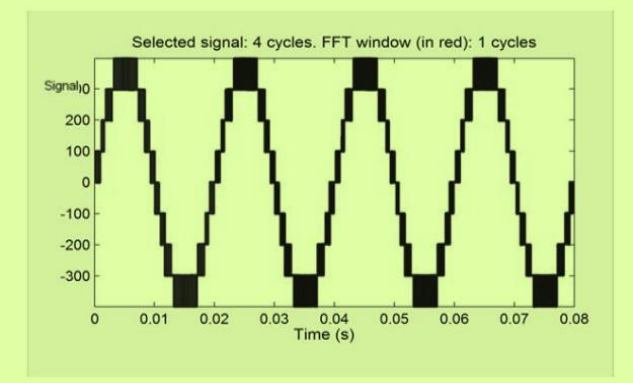

Fig. 6: Output phase voltage waveform for asymmetric (9-level) MLI using IPD-CLSPWM

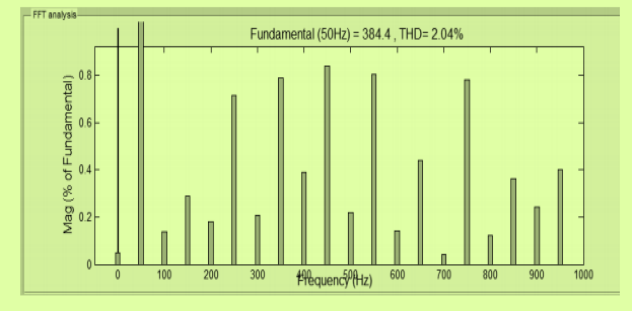

Fig. 7: FFT analysis of voltage waveform of asymmetric (9-level) cascaded MLI using IPD-CLSPWM

V. Simulation and Result

This section show the comparative study of output voltage of 9-level asymmetrical cascaded multilevel inverters cascaded is compare for the PD, POD, APOD methods ,and it also shows the THD profile and performance of the circuit with IM for three PWM techniques, Cascaded multi-level inverter shows the lowest THD profile with no any type of filter and also any category of dependency of inductor and capacitor used for smooth the current wave form and due to less number of switching devices gate firing circuit also reduced that's why whole cost and presentation has been increased .

System Parameters	IPD	POD	APOD
THD (%)	2.04 %	6.09%	THD 2.09%

Table 2: The THD of the output voltage of 9-level ACMLI with IM Compared for IPD, POD, and APOD

9-LEVEL			
Switching techniques	IPD	POD	APOD
Voltage THD%	2.04%	6.09%	2.09%

Table 2: THD of output voltage of 9- level ACHB

VI. Conclusion

In this paper the multicarrier pulse width modulation (PWM) procedure for 9-level have been presented. Performance factor similar to total harmonic distortion (THD) of the output voltage of asymmetric cascade multi-level inverter (CMLI) have been evaluate, presented and analyzed. The total harmonic distortion (THD) of the output voltage of unstable cascade multi-level inverter CMLI) is studied below different techniques such as IPD, POD & APOD, best for 9-level multi-level inverter (MLI).

Therefore, it concluded that the 9-level cascade multi-level inverter (CMLI) present a lower percentage total harmonic distortion (THD) The harmonic distortions present in the output voltage waveforms were experiential and calculate from side to side Fast Fourier Transform (FFT) analysis tool in Matlab and Simulink.

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