Design & Comparative Analysis of High Speed & Low Power 8x8 bit Radix-4 Booth Multiplier

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Abstract— Multiplication is essential operation for any high speed digital logic system design, digital signal processors or control system. Primary issues in design of multiplier are area, delay, and power dissipation. Many design architectures and techniques have been developed to overcome these issues. This paper mainly presents radix-4 booth multiplier using Booth encoder, Booth decoder, Sign extension and Carry Look-ahead Adder (CLA) blocks. Keeping in mind that power dissipation and delay are the primary factors for multiplier and it should be improved in the design. The design has been implemented using PTM 45nm CMOS technology at 1.0v supply voltage in TANNER EDA V.15 tool. The results are compared with previously reported papers.

Key words: Booth Multiplier Algorithm, Radix 4 Modified Booth Multiplier, Simulation Results, Comparison

I. INTRODUCTION

This paper presents an efficient implementation of high speed Multiplier using the shift and adds method, Radix-4 modified Booth Multiplier algorithm. The parallel Multipliers like Radix 2 and Radix 4 modified booth Multiplier does the computations using lesser adders and lesser iterative steps. As a result of which they occupy lesser space as compared to the serial Multiplier. This is very important criteria because in the fabrication of chips and high performance system requires components which are as small as possible. [12] When consider Radix-2 algorithm it sees some points. Radix-2 has certain limitations but it is useful for understanding the Radix-4 concept.

Now The A.D Booth observed that

- Whenever there was a large number of consecutive ones, the corresponding additions could be replaced by a single addition and a subtraction
- The longer the sequence of ones, the greater the savings.
- The effect of this translation is to change a binary number with digit set [0, 1] to a binary signed-digit number with digit set [-1, 1].

The following gives the algorithm for performing sign and unsigned multiplication .Operations by using Radix-4 Booth recoding.

Algorithm: (for unsigned numbers)

- Pad the LSB with one zero
- Pad the MSB with two zeros if n is even and one zero if n is odd
- Divide the Multiplier into overlapping groups of 3-bits
- Determine partial product scale factor from modified Booth-2 encoding table
- Compute the multiplicand multiplies
- Sum partial products
- Algorithm: (for signed numbers)
- Pad the LSB with one zero
- If n is even don't pad the MSB (n/2 PP's)
- Divide the Multiplier into overlapping groups of 3-bits
- Determine partial product scale factor from modified Booth-2 encoding table
- Compute the multiplicand multiplies
- Sum partial products

Booth recoding is fully parallel and carry free. It can be applied to design a tree and Array Multiplier, where all the multiples are needed at once. Radix-4 Booth recoding system works perfectly for both signed and unsigned operations.

To understand the Radix based multiplication it is necessary to know Radix-2 and its truth table which is shown below.

Yi	Yi-1	Zi	Explanation
0	0	0	No string of 1s in sight
0	1	1	End of string of 1s in Y
1	0	1	Beginning of string of 1s in Y
1	1	0	Continuation of string of 1s in Y

Table 1: Radix-2 Booth Recoding

In this algorithm the current bit is Yi and the previous bit is Yi-1 of the Multiplier Yn-1Yn-2…… Y1 Y0 are examined in order to generate the ith bit Zi of the recoded Multiplier Zn-1 Zn-2…….Z1 Z2. The previous bit Yi-1 serves only as the reference bit. The recoding of the Multiplier bits need not be done in any predetermined order and can be even done in parallel for all bit positions. [17] The observations obtained from the Radix-2 Booth recoding are shown below:

- It reduces the number of partial products which in turn reduces the hardware and delay required to sum the partial products. It adds delay into the formation of the partial products.
- It works well for serial multiplication that can tolerate variable latency operations by reducing the number of serial additions required for the multiplication.
- The number of serial additions depends on the data (multiplicand)
- Worst case 8-bit multiplicand requires 8 additions.
- 01010101 ⇔ 1 -1 1 -1 1 -1 1 -1.

II. MODIFIED BOOTH ALGORITHM

The modified booth algorithm can be of different types. Radix based modified booth encoding Multipliers are Radix-4, 8, 16, 32 and all of have its advantages and disadvantages. The Radix-2 disadvantages can be eliminated by examining three bits of Y at a time rather than two. The modified Booth algorithm is performed with recoded Multiplier which multiplies only +-a and +-2a of the multiplicand, which can be obtained easily by shifting and/or complementation. The truth table for modified Booth recoding is shown below:

Yi+1	Yi	Yi-1	Zi+1	Zi	Zi/2	Explanation

0	0	0	0	0	0	No string of 1s in sight
0	0	1	0	1	1	End of strings of 1s
0	1	0	0	1	1	Isolated 1
0	1	1	1	0	2	End of string of 1s
1	0	0	-1	0	-2	Beginning of string of 1s
1	0	1	-1	1	-1	End a string, begin a new one
1	1	0	0	-1	-1	Beginning of string of 1s
1	1	1	0	0	0	Continuation of string of 1s

Table 5.2: Radix-4 Booth Recoding

Booth encoding multiplication is able to reduce the number of partial product and increase the speed of binary multiplication. Radix-4 booth Multiplier reduces the number of partial product by half N/2. Booth recoding is fully parallel and carry free. It can be applied to design a tree and Array Multiplier, where all the multiples are needed at once. Radix-4 Booth recoding system works perfectly for both signed and unsigned operations.

III. RADIX-4 PROPOSED BOOTH MULTIPLIER ARCHITECTURE

Multiplier architecture has been shown in the figure1 This architecture consist of some blocks like Booth encoder, Booth decoder, Sign extension and Carry Look-ahead Adder(CLA) blocks and finally gets the output. The numbers of inputs X are applied to the booth encoder where it generates the select signals for each bit of multiplicand. The decoder block generates the partial product from the selector signal which is generated from the booth encoder. Here also used half adder with the decoder circuit for the 2's complement for the negative cases. This sign bit extension is different from the reference value, so in this paper the highest partial product bit is applied rather than the multiplicand bit. This difference maybe come from so take a different approach to add sign bit. In reference paper the sign bit is always put at adder part. Also finish this target at the generation partial product. Finally the output goes to CLA (Carry Look-ahead Adder) and then have the appropriate answer of Multiplier.

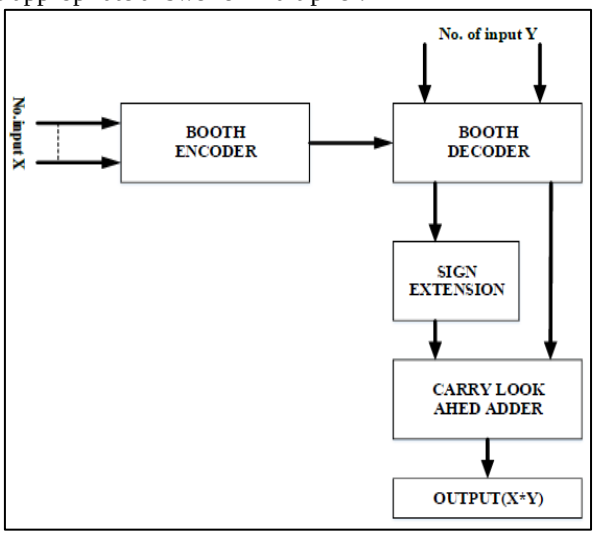

Fig. 1: Radix-4 Proposed Booth Multiplier Architecture

IV. 8X8 BIT RADIX-4 BOOTH MULTIPLIER SCHEMATIC AND SIMULATION

The simulation of the 8x8 bit modified Radix-4 Multiplier and is done in the TANNER tool. In this simulation consider the 45nm parameter and the given VDD is 1v. The figure 2 shows the complete schematic view of the Multiplier and figure 3 shows the simulated result of Multiplier. With the help of simulation the different parameters like power dissipation, delay and number of transistors are easily find and they are compared with the other existing Multipliers. Simulation gives the output of Radix-4 with the appropriate input. For the multiplication here consider 11111111 bits for multiplicand and 11111111 bits for Multiplier and the final output is 1111111000000001.

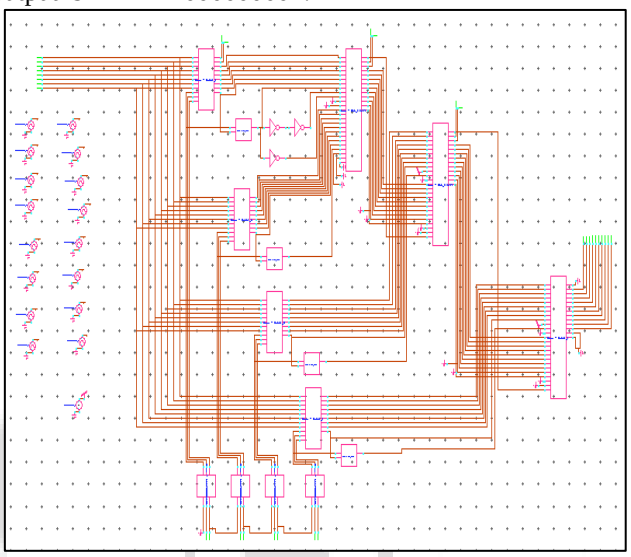

Fig. 2: Schematic of 8x8 bit Radix-4 Booth Multiplier

For the Radix-4 booth Multiplier it has been seen that the overall area is much less as than other Multipliers. From the blocks discussed above an 8x8 modified Booth Multiplier was constructed following the architecture. The final schematic of the modified Booth Multiplier is shown in Figure 3. The delay is measured at 447.14ps.

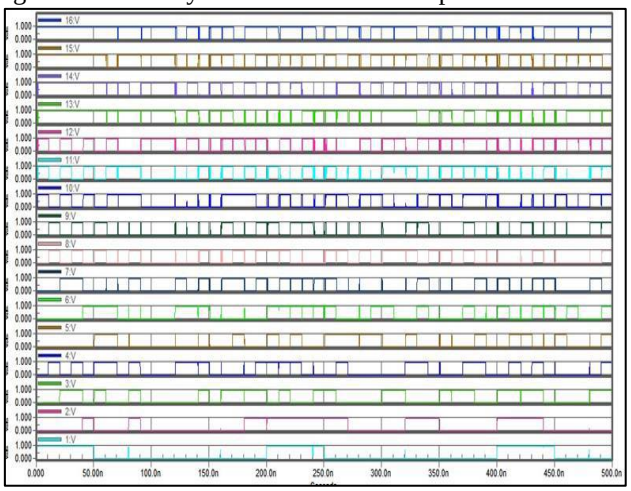

Fig. 3: Simulation of 8x8 Bit Radix-4 Booth Multiplier

V. COMPARISONS OF 8X8 BIT MULTIPLIERS WITH RADIX-4 BOOTH MULTIPLIER

The Radix-4 modified booth Multiplier is designed with the new technology and proposed architecture become successful for the delay, power dissipation and area means number of transistors

Parameters	Proposed Radix-4 Multiplier	[2]			[10]
VDD	1V	3.5V	2.5V	2.0V	---
Delay	447.14 (ns)	1.21 (ns)	0.742 (ns)	0.135 (ns)	3.75 (ns)
Power	1.00 (mW)	8.08 (mW)	4.03 (mW)	1.41 (mW)	324.5 (uW)
Technology	45 nm	350 nm	250 nm	180 nm	130 nm

Table 5.5: Comparisons of 8x8 Bit Multipliers with Radix-4 Booth Multiplier

VI. CONCLUSION

In this paper, a deep detailed study of 8x8 bit Radix-4 Booth Multiplier is carried out. Multiplier very important in DSP (Digital Signal Processing) and Math processors so it should be faster and here tried to make this thing possible. The design has been implemented using PTM 45nm CMOS technology at 1.0v supply voltage in TANNER EDA V.15 tool. Also it has very low power dissipation compared to other Multipliers because in the Radix-4 the partial product were generated using booth recoding which is much faster than conventional partial product generation. The power dissipation of 1.0 mW and a delay of 447.14 ns has been observed for Proposed 8x8 bit Radix-4 Booth Multiplier. This achieved result was good than previously reported papers.

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