Design & Implementation of High Speed & Low Power Wallace Multiplier

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Abstract— 8x8 bit Multiplier architecture based on Wallace Tree, which is efficient in terms of power and regularity without increase in delay and area. The idea involves the generation of partial products in parallel using AND gates. The addition of partial products is done using Wallace tree, which is hierarchal, divided into levels. There will be a reduction in the power consumption, since power is provided only to the level that is involved in computation. The proposed 8x8-bit Wallace tree Multiplier has been designed using proposed compressors and the power consumption results are low and also less delay has been observed. The proposed Wallace tree Multiplier using these compressors achieves significant amount of less power than conventional Wallace tree Multiplier. The designs are implemented and power results are obtained using TANNER EDA 15.0 v tool.
Key words: Flow of Wallace Tree, 8X8 Bit Wallace Architecture, Simulation Results, Comparison

I. INTRODUCTION

Several popular and well-known schemes, with the objective of improving the speed of the parallel Multiplier, have been developed in past. In 1964, C.S. Wallace observed that it is possible to find a structure, which performs the addition operations in parallel; thus resulting in less delay. A Wallace tree is an implementation of an adder tree designed for minimum propagation delay. Rather than completely adding the partial products in pairs like the Ripple adder tree does, the Wallace tree sums up all the bits of the same weights in a merged tree. [11]

A Wallace tree is an efficient hardware implementation of a digital circuit that multiplies two integers. The Wallace tree has three steps:

- Multiply (ANDing) each bit of one of the arguments, by each bit of the other Depending on position of the multiplied bits, the wires carry different weights.
- Reduce the number of partial products with two by layers of full and half adders.
- Group the wires in two numbers, and also add them with a conventional adder.
- The second phase works as follows. As long as there will be three or more wires with the same weight then add a following layer:
- Take any three wires with the same weights and input them into a full adder. The result is in an output wire of the same weight and an output wire with a higher weight for each three input wires.
- If there are two wires for the same weight left, input them into a half adder.
- If there is just one wire left, connect it to the next layer.
- Wallace introduced a different way of parallel addition of the partial product bits using a tree of carry save adders, which is known as "Wallace Tree".

In order to perform the multiplication of two numbers for the Wallace method, partial product matrix is reduced to a two-row matrix with using a carry save adder and the remaining two rows are added a fast Carry-Propagate Adder (CPA) to form the product. This advantage becomes more pronounced for Multipliers of bigger than 16 bits. Wallace tree flow can be seen in Figure 1.

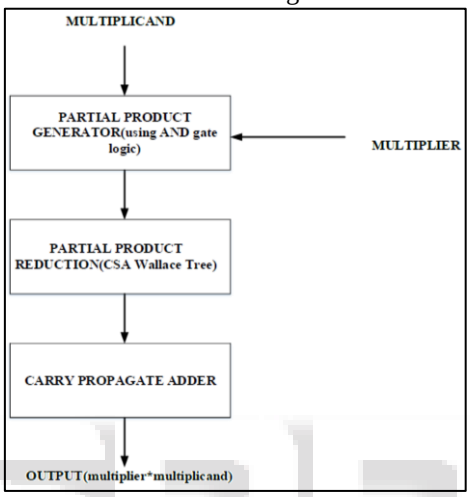

Fig. 1: Flow of Wallace Multiplier

Wallace Tree architecture, all the bits of all of the partial products in each column are added together by a set of compressors in parallel without propagating any carries. Another set of compressors then reduces this new matrix and so on, until a two-row matrix is generated. Here a 3:2 compressor is used. Then, a fast adder is used at the end to produce the final result. The advantage of Wallace tree is speed.

Wallace method uses three-steps to process the multiplication operation

- Formation of bit products
- The bit product matrix is reduced to a 2-row matrix by using a carry-save adder
- The remaining two rows are summed using a fast carry-propagate adder to produce the product.
- In general, its multiplication process can be summarized as follows:
- After generating the partial products, a set of counters reduces the partial product matrix but it does not propagate the carries.
- The resulting matrix is composed of the sums and carries of the counters.
- Another set of counters then reduces this matrix and the whole process continues until a two- row matrix is generated.
- The two rows get summed up with a final adder, preferably by a carry Propagate Adder (CPA). This method takes advantage of the Carry Save Architecture in order to avoid the Carry Propagation until the final

adder. In this scheme, the number of levels is crucial since they determine the speed of the Multiplier.

II. IMPLEMENTATION OF 8X8 BIT WALLACE MULTIPLIER

The power management has become a great concern due to the increased usage of multimedia devices. Multipliers are the main sources of power consumption in these devices. The 3:2, 4:2 and 5:2 compressors are the basic components in many applications like partial product summation in Multipliers. In this Thesis, These types of compressors are designed. Different logic styles of XOR-XNOR gates and Multiplexers have been implemented. The implementation of XOR-XNOR gates and multiplexer circuits achieves low power with less number of transistor counts. The proposed compressor architecture can be built using combinations of XOR-XNOR gates and multiplexer circuits. The performance of basic compressor architectures with these low power XOR-XNOR gates and multiplexer blocks is found to be efficient in terms of area and power. Hence, the proposed 8x8-bit Wallace tree Multiplier has been designed using this proposed compressors and the power results are good and also delay. [9] The proposed Wallace tree Multiplier using these compressors achieves significant amount of less power than conventional Wallace tree Multiplier. The designs are implemented and power results are obtained using TANNER EDA 15.0 v tool.

8x8 bit Multiplier architecture based on Wallace Tree, which is efficient in terms of power and regularity without increase in delay and area. The idea involves the generation of partial products in parallel using AND gates. The addition of partial products is done using Wallace tree, which is hierarchal, divided into levels. There will be a reduction in the power consumption, since power is provided only to the level that is involved in computation. To improve the speed of addition at the third level of computation, Carry Propagate Adder (CPA) is proposed. The 8x8 bit size is chosen since Wallace Tree gets its performance improvement at the operand width higher than four do.

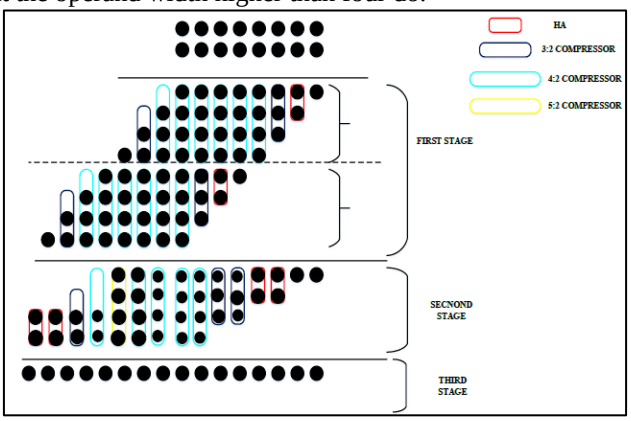

Fig. 2: 8X8 bit Wallace Architecture

The proposed High Speed (HS)-Wallace tree Multiplier uses 4:2 and 5:2 compressor structures for the partial product addition in the final stage of product accumulation stage. The hierarchical decomposition of an 8x8 Wallace tree Multiplier based on proposed methodology shown in figure 2. The 8 partial product rows generated are grouped and added in parallel .These partial products are divided into groups, where each group contains four adjacent rows of partial products. The addition operation in the columns of each block can be performed by choosing either half adder or full adder or 4:2 compressors or 5:2 compressors according to the number of bits to be added. This represents the first level of computation. The partial sums thus generated are again appropriately divided and added again in the same manner, forming the second level, third level and so on till it has two rows, one with sum and other with carry of previous column. [5] In the final stage, here perform addition using Carry Propagate Adder (CPA) to reduce the delay due to carry propagation.

III. 8X8 BIT WALLACE MULTIPLIER SCHEMATIC & SIMULATION

A fast process for multiplication of two numbers was developed by Wallace. By using the Wallace method, a three step process is used for the multiplication of two numbers; the partial products are formed using the AND gate. The bit product matrix are reduced to a two row matrix, where sum of the row equal to the sum of bit products, and two resulting rows of the bit product are summed with a fast adder(compressor) to produce a final product. In the Wallace Tree method, three single bit signals are going to a one bit full adder which is called a three input Wallace Tree circuit, and the output signal (sum) is given to the next stage full adder of the same bit, and the carry output signal thereof is going to the next stage full adder of the same no of bit, and the carry output signal thereof is supplied to the next stage of the full adder located at a one bit higher position.

For the multiplication here consider 11111111 bits for multiplicand and 11111111 bits for Multiplier and the final output is 1111111000000001.

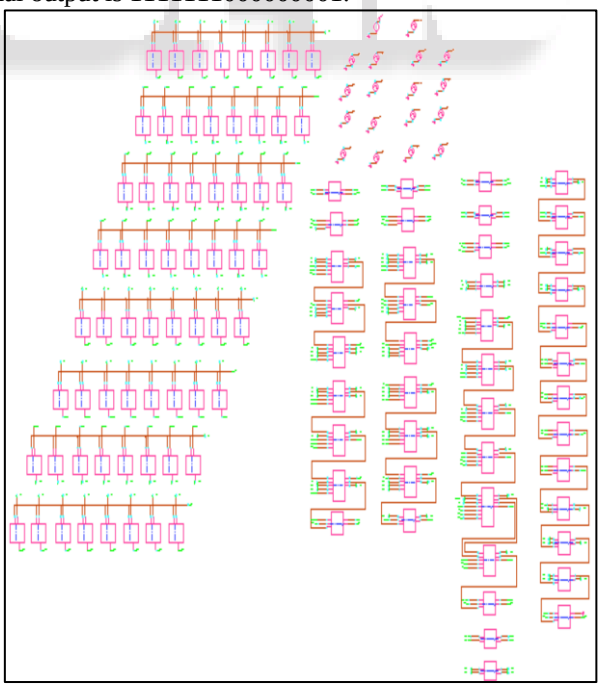

Fig. 3: Schematic of 8x8 Bit Wallace Multiplier

Schematic diagram of 8x8 bit Wallace Multipliers shown in figure 3. This Multiplier has one of the tendency that it is more complicated compared to rest of the two Multipliers although very much useful as far as delay is concerned.

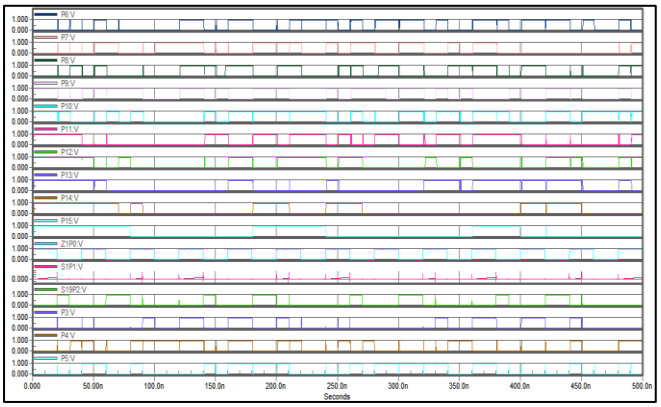

Fig. 4: Simulation of 8x8 bit Wallace Multiplier

IV. COMPARISONS OF 8X8 BIT MULTIPLIERS WITH WALLACE MULTIPLIER

Comparisons of Wallace Multiplier with other 8x8 bit Multiplier is shown in table 1. With this comparisons proposed Wallace Multiplier gets better in terms of power and speed.

Parameters	Proposed Wallace Multiplier	[10]	[12]
VDD	1V	-	1.2V
Delay	124 (ps)	2.81 (ns)	21.711 (ns)
Power	275.85 (uW)	5.39 (mW)	157.65 (mW)
Technology	45 nm	180 nm	-

Table 1: Comparison of 8x8 bit Multiplier with Wallace Multiplier

V. CONCLUSION

In this paper, the implementation and analysis of a novel Wallace tree architecture is proposed. Simulations have been carried out for that and comparative analysis has been done. The comparison result also shows that a significant reduction of power is achieved. At an operating voltage of 1.0V, the power has been observed to be 275.85uW and a delay of 124 ps has been observed. The results prove that the proposed architecture is more efficient than the conventional one in terms of Power consumption and latency. Wallace Multiplier is much faster than other two Multipliers. The overall it could say that for the faster multiplication Wallace is better than other twos because of its speed and low power.

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