CMOS Design & Analysis of Receiver System in Satellite Communication using 180 nm Technology

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Abstract— This project describes the complete design of a low-cost 14 GHz Receiver front-end in 180 nm technology. It covers the topics of a system plan, designs of building blocks, designs of application-boards and real environment tests. A homodyne architecture with a 500 MHz IF. The design of a LNA in Radio Frequency (RF) circuit requires the trade-off in many importance characteristics such as gain, Noise Figure (NF), stability, power consumption and complexity. Expressions developed will help circuit and system designers to come to an optimum power consumption versus performance trade-off. An RF receiver front-end Receiver systems is designed. The receiver occupies only 0.35 mm2 in a 0.18 µm CMOS process, consists of a low-noise amplifier, downconverter and a low pass filter. The measured receiver gain is 21 dB, Noise Figure is less than 5 dB, input IIP3 is -5 dBm and the receiver consumes 19.5 mW from a 1.8V supply. The receiver covers all the bands from 13 GHz to 15 GHz.

Key words: LNA, Mixer, LPF

I. INTRODUCTION

Now-a-days portable wireless communication systems have experienced tremendous growth. The design of ultralow power radio frequency (RF) transceivers is vital to the existence of such wireless sensor networks. Some of the important issues for developing components of wireless communications systems are low power and highly integrated circuits(IC). To the present technology, there is a high demand for RF receiver IC design that has low power consumption, high sensitivity and wide dynamic range, and also to reduce the number of off-chip passive components in the circuit.

This paper describes about the design of 14 GHz CMOS Receiver for satellite communication. The successive approach is to combine and co design of two or more receiver blocks in a single block and thus saving the power by reusing the bias currents. In the RF receiver system, "front-end" is a generic for all the receiver blocks between the antenna and the intermediate frequency (IF) stage.

Section II invokes the design parameter of Low Noise amplifier (LNA) with its design equation. Section III serves the design of mixer and Low Pass Filter and its development. Section IV shows the integration of LNA, Mixer and LPF in the aspect of receiver front end block into a single IC chip. Section V illustrates the performance and analysis of Receiver chip.

II. LNA DESIGN

The low noise amplifier (LNA) is the first building block of wireless receiver section and for its unique feature towards compensating optimum noise figure with high gain. There are different topologies involved in LNA design. In our design Cascoded Common Source (CS) topology with source degeneration technique is employed. The transistor M2 is connected in common gate connection and the transistor M1 is connected in common source connection. Together they form a cascode, this cascode connection is necessary to provide the required isolation between the input and the output, reduce the effect of miller effect caused by gate-drain capacitance Cgd of the M1 transistor.

The main aspect of designing LNA is to match antenna impedence (generally 50Ω) for maximum power transfer with optimum noise figure and also high gain.

The specifications of LNA which is designed

Operating Frequency range – 12 GHz – 16 GHz
Noise Figure < 5 dB
Gain > 10 dB
S-Parameter
S11
S21
S22
Technology – 0.180 µm CMOS
Supply Voltage – 1.8 v

Design parameters and its equations

1) Step 1:

For optimum Noise figure ,width is to be manipulated

W_opt=1/(〖3C〗_ox ωLR_s)=30 µm

Where C_ox – Permittivity of Gate oxide = 8.42*〖10〗^(-3) F/m^2
R_s - Source impedence = 50 Ω
ω - Angular Frequency
L – Length of Channel

2) Step 2:

Using small signal analysis the impedence matching equation was solved into

R_s=(gm Ls)/C_gs =50 Ω
Ls=(C_gs R_s)/gm =189.8 pH

Where – gm – Transconductance
Ls - Source Inductor
C_gs- Gate source capacitance = (〖〖2C〗_ox W〗_opt L)/3

3) Step 3:

For frequency tuning Gate inductance is to choosed

L_g=1/C_gs (1/ω-L_s C_gs) = 2.37 nH

Figure 3.2 Schematic of LNA using Cadence EDA

III. MIXER & LPF DESIGN

An ideal double balanced mixer simply consists of a switch driven by the local oscillator that reverses the polarity of the RF input at the LO frequency[1]. To get the highest performance from the mixer we must make the RF to IF path as linear as possible and minimize the switching time of the LO switch. The ideal mixer would not be troubled by noise (at the low end of the dynamic range) or intermodulation

distortion (IMD) at the high end since the transconductors and resistors are linear and the switches are ideal. The ideal balanced structure cancels any output at the RF input frequency since it will average to zero. It also cancels out any LO frequency component since we are taking the IF output as a differential signal and the LO shows up as common mode. Therefore, to take full advantage of this design, an IF balun, either active (a differential amplifier) or passive (a transformer or hybrid), is required.

The specifications of Mixer which is designed

RF Frequency – 14 GHz

Local Oscillator Frequency (LO) – 14.5 GHz

Intermediate Frequency (IF) – 500 MHz

Technology – 0.180 µm CMOS

Supply Voltage – 1.8 v

Design parameters and its equations

1) Step 1:

With voltage gain goal of 6dB we can calculate gm

Conversion gain, C.G = 〖10〗^(6⁄10)=3.98

gm=2/Π R_L/V_gain - R_S = 0.0142

2) Step 2:

The RF Mosfet must ensured with the width calculation

W=(gm^2 L)/(2 K_p I_ds)=105 µm

The specifications of LPF which is designed

Cut-off Frequency = 500 MHz

Due to design constrains in IC Fabrication, it is better to reduce inductor usage because it consumes large chip area. So we will go for Π - Filter

Design parameters and its equations

Π -Filer comprises of one series inductor and two parallel capacitors

3) Step 3:

The inductor value is to be choosen

L=Z_0/ΠF =30 nH

The capacitor value is to be choosen

C=1/(ΠZ_0 f) = 1270 fF

Figure 3.4 Schematic of Mixer using Cadence EDA

IV. INTEGRATION OF RECEIVER CHIP

It becomes more efficient in sake of IC integration rather than discrete components, the advancements are

Speed

Size Cost

Power Consumption

Figure 3.6 Schematic of Receiver using Cadence EDA

V. PERFORMANCE ANALYSIS

The Integrated Receiver front-end has been designed in CadenceVirtuoso design environment, simulated using Cadence Spectre and synthesized with CMOS 180 nm technology standard cell library.

VI. CONCLUSION

In this work, the Receiver front-end unit is designed and simulated. Experimental results of the designed Receiver confirm that there is a significant reduction in Noise Figure and optimum Gain. Thus the Receiver is suitable for high Noise reduction applications such as ISM band, satellite communication and RF applications.

REFERENCES

[1] Yu Lin Wei and Jun De Jin, "A low power low noise amplifier for K-band applications," IEEE Microwave and Wireless Components Letters,vol. 19, no. 2, pp. 116-118, Feb. 2012.

[2] Hsieh Hung Hsieh, "A 40 GHz low noise amplifier with a positive-feedback network in 0.18µm CMOS," IEEE Trans. On MicrowaveTheory and Techniques, vol. 57, no. 8, pp. 1895-1902, Aug.2009.

[3] Viranjay M. Srivastava, K. S. Yadav, and G. Singh, "Design and performance analysis of doublegate MOSFET over single-gate MOSFET for RF switch," Microelectronics Journal, vol. 42, no. 3, pp. 527-534,March 2011.

[4] Nazif Emran Farid, Arjuna Marzuki, & Ahmad Ismat,"A variable gain 2.5 GHz CMOS low noise amplifier for mobile wireless communications,"Proc. of 9th IEEE Int. Conf. of communications, Kuala Lumpur,Malaysia, 15-17 Dec. 2009, pp. 885-889.

[5] Ming Hsien Tsai, S. Hsu, Fu Lung Hsueh, Chewn Pu Jou, Sean Chen, and Ming Hsiang, "A wideband low noise amplifier with 4 kV HBM ESD protection in 65 nm RF CMOS," IEEE Microwave and Wireless Components Letters, vol. 19, no. 11, pp. 734-736, Nov. 2009.

[6] Fu Lung Hsueh, Chewn Pu Jou, Sean Chen, and Ming Hsiang, "Gilbert Mixer with 4 kV HBM ESD protection in 65 nm RF CMOS" IEEE Microwave and Wireless Components Letters, vol. 19, no. 11, pp. 734- 736, Nov. 2009IEEE Trans. on Microwave Theory and Techniques, vol. 57, no. 2, pp. 298-305, Feb. 2015.

[7] Tom yum gong in Wei and Jun De Jin, "A low power Gilbert cell mixer for Ku-band applications," IEEE Microwave and WirelessComponents Letters, vol. 19, no. 2, pp. 116-118, Feb. 2012.

[8] Parssinen, J. Jussila, J. Ryynanen, L. Sumanen, K. Halonen, "A 2- GHz Wide-Band Direct Conversion Receiver for WCDMA Applications",IEEE Journal of Solid-State Circuits, vol 34, pp. 1893-1903, Dec 1999.

[9] Rofougaran, G. Chang, J. Rael, J. Chang, M. Rofougaran, P. Chang, M. Djafari, J. Min, E. Roth, A. Abidi, H. Samueli, "A Single-Chip 900-MHz Spread-Spectrum Wireless Transceiver in 1-um CMOS"

