

VLSI Realisation of Multipliers for Signal Processing Applications

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Abstract— Multipliers plays an important role in many computation systems. Multipliers in VLSI require more hardware resources and more processing time and are used in digital processing systems. There are many researches in multiplier that result in reducing the power and thereby, causing delay. Generation of partial products in multipliers may result in large power consumption. Multipliers are used in applications such as DSP, FFT etc., they require large chip area. Normally array multiplier is based on its regular structure and it is compared with vedic multiplier. Though vedic multiplier work faster in all aspect with respect to other multipliers. Here in this work vedic multiplier is designed using tanner tool and perform spice simulation such as wave form and design rule.

Keywords: VLSI Realisation, Multipliers

I. INTRODUCTION

Multiplier is one of the key component in arithmetic and logic unit. Higher throughput arithmetic operations are important to achieve the desired performance in many real time signal and image processing applications. In multiplier power dissipation and speed are the most important parameter. The main disadvantage of the multiplier is the worstcase delay. Which leads to reducing the time delay as well as the path delay. Digital signal that travel from input of logic gate to that of the output gate will cause delay due to the minimum switching activity ie., the total number of signal transition of the system. The low power will reduce the complexity, execution time and power which can overcome the drawback of other multiplier.

II. ARRAY MULTIPLIER

Array multiplier is well known due to its regular structure. Multiplier circuit is based on addition and shift algorithm. It can also perform serial and parallel multiplication. The composition of an array multiplier is shown in figure 1.

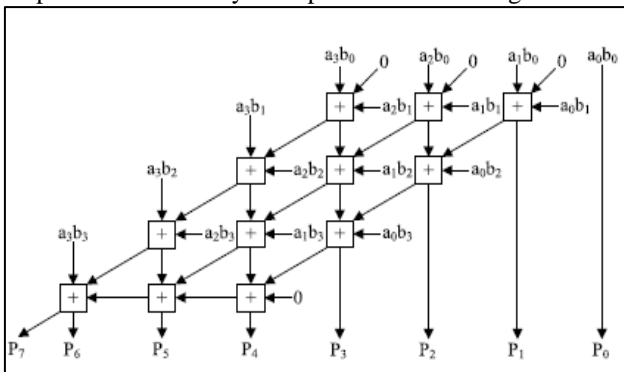


Fig. 1: Normal Array multiplier

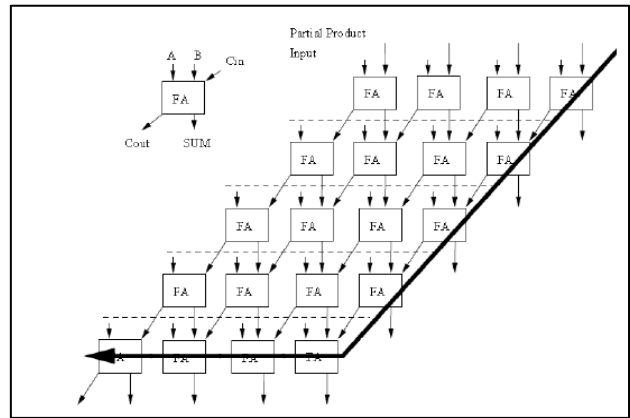


Fig. 2: Array Multiplier 4X4

The overall structure of an array multiplier can easily be compacted into a rectangle, resulting in a very efficient layout. Normally array multiplier works with XILINX software by Verilog code in FPGA kit determination of the propagation delay in array multiplier is not a straightforward. Consider the implementation of the partial product in sum adders are implemented as ripple carry adder. The timing path is required for optimization and that leads large path of almost identical length can be identified. An approximate expression for the propagation delay.

$$t_{mult} = [(M-1) + (N-2)]t_{carry} + (N-1)t_{sum} + t_{and} \quad (1)$$

where t_{carry} is the propagation delay between input and output carry, t_{sum} is the delay between the input carry and sum bit of the full adder, and t_{and} is the delay of the AND gate. Carry select adder does not make much sense from that of design stand point. So we use we use ripple carry adder. From the above equation it can be deduced that minimum value of t_{mult} will result in the minimum value of t_{carry} and t_{and} . The critical path can be determined and it has same length.

III. RELATED WORK

A brief review of all the following papers has been done and the work of the following authors is as written below. These papers describes about left to right Design of Array Multiplier using CMOS logic.

Asati and A.Chandrasekar present the paper on design of array multiplier in which they designed the multiplier with logic that is CMOS logic.

They discussed the latch up problem occurred in CMOS devices and their preventions. Another The Multiplier designed with the Cadence Simulator that simulates the design using with 180nm technology for CMOS. Results shown that a proposed CMOS have better performance in terms of delay than the CMOS, as delay for 4*4 multiplier using CMOS logic is 7.888 ns and using BiCMOS logic it is 6.388 ns [1]. Kripa Mathew, S.AshaLatha, T.Ravi, E.Logashanmugam during this paper planned for minimize the transistor count in adder cell for more efficient in terms

for area, power and delay. With this less transistor count in adder cell, the proposed array multiplier performance increases using 10T compared with the conventional array multiplier using 16T full adder cell. The design is simulated using 32nm and 130nm CMOS technology.

For 32nm CMOS technology, the proposed design uses 96 less transistor count and saves 2.82% of total power, 13.24% of more speed and 15.69% less power delay product [2]. N.Ravi, A.Satish, Dr.T.Jayachandra Prasad and Dr.T.SubbaRao worked on the design of Array Multiplier with trade of in power and area for the same. In this paper, the proposed 4x4 multiplier, to add carry bits without using Ripple Carry Adder (RCA) in the final stage. Due to this the multiplier shows 56 less transistor count which cause trade off in power and area. For 180nm technology the proposed multiplier has shown 13.91% less power, 34.09% more speed and 59.91% less energy consumption and to compute the multipliers performance same design is simulated with different technologies.

IV. VEDIC MULTIPLIER

Vedic mathematics is derived from ancient Atharvana Veda. It consists of 16 different sutras which describe different mathematical calculations. Vedic mathematics is mainly word formulae and these sixteen principles are termed as sutras. Vedic multiplier which has digital multiplier architecture based on the Urdhva Triyakbhyam sutra is otherwise termed as “Vertically and Crosswise” algorithm. The Vedic algorithm Urdhva Triyakbhyam sutra is the most preferred one in the multiplication process.

The design of vedic multiplier is most convenient and fast processing systems involving decimal number multiplication. It increases the speed of the processor and reduces the delay in the system. The multiplier operates fastly when all the partial products in vedic multiplier are generated in parallel. By using vedic multiplier, the number of NAND gates, Half adders and Full adders can be reduced. Normally vedic multiplier is independent of frequency as all the partial products and sums are generated in parallel. The net advantage of vedic multiplier is that there is no need of higher clockfrequencies and large chip size. Vedic multiplier is very much efficient in area, speed and power consumption.

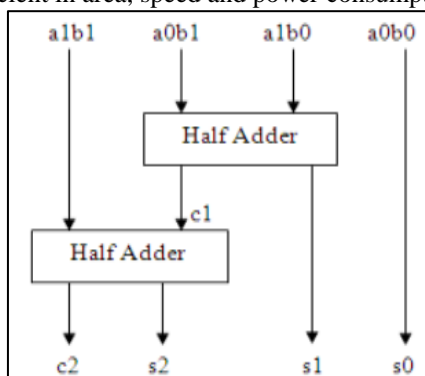


Fig. 3: 2x2 Vedic Multiplier

In recent years, low delay in the circuit design is crucial issue in many systems. Adiabatic logic circuit dissipates less power and load capacitance is recovered than static CMOS logic. It has become a significant approach in low power circuit design and with 8x8 CMOS transistor. A

high speed vedic multiplier has low energy consumption in VLSI design and has become the key hardware component in many processors. Vedic multiplier is very faster than other conventional multiplier. Among the different sutras present Urdhva Triyakbhyam sutra is used in this paper. The Urdhva Triyakbhyam sutra is an ancient Indian multiplication which has the simple multiplication structure. As the energy is recovered when it is transferred to the load and thus leads to low power consumption. The proposed multiplier structures have been designed in 0.13 micrometer CMOS technology and has been verified by transistor level realization.

The performance and the efficiency of the processor is mostly based on the speed of the system. High speed processor is recommended by most of the arithmetic computation system. Multiplier. In Multiplier many computations are performed and has high throughput. So high speed multiplier are generally used in VLSI technology. This paper mainly focuses on Ultra high speed multiplication processing Vedic Mathematics.

Some multipliers like booth multiplier, Modified Booth Multiplier, Wallace tree multiplier, dadda multiplier and array multipliers were considered for high speed multiplication. But in these multipliers many intermediate steps are involved. This leads to reduction in speed and high processing time. For any digital signal processing and image processing systems multiplier is the essential and better realization for the above application. For any multiplication operation the speed and efficiency of the multiplier is a constraint. So thereby reducing the steps involved in upcoming computation an increase in speed and low power consumption can be achieved. In most of the systems, the efficiency is determined by the speed of the multiplier. Energy efficiency and area efficiency is more important for high performance applications.

For low power dissipation heavy, expensive cooling machines and heat sinks, and fans are required to maintain the low power consumption. Many power management techniques have been employed to reduce the power dissipation in multiplier. Scaling plays an important role in multiplication in computation processor. As the technology scales down below 90nm, then it becomes more difficult in voltage supply. Scaling in voltage supply may reduce power delay in the transistor. By using adiabatic technique the power dissipation in CMOS circuits and various processor can be reduced. The energy dissipated in PMOS network can be reduced. Vedic multiplications can be implemented in tanner software by which S-edit and W-edit can be taken. The variation in parameters highly effect the multiplication technique.

V. VEDIC 4X4 BIT MULTIPLIER

The 4x4 bit Vedic multiplier is implemented by using four 2x2 bit Vedic multiplier. To illustrate, 4x4 bit Vedic multiplication, it have $A=A_3A_2A_1A_0$, $B=B_3B_2B_1B_0$ and the output is $S_7S_6S_5S_4S_3S_2S_1S_0$. Let's A and B is divided into two parts A_3A_2 & A_1A_0 for A and B_3B_2 & B_1B_0 for B by using the basic of Vedic multiplication, taking the two bit simultaneously in the circuit by using 2 bit multiplier block. Here “Urdhva-Triyakbhyam” (Vertically and Crosswise) sutra is used to propose such an architecture for the

multiplication of 2 binary numbers. The beauty of Vedic multiplier is that here partial product generation and additions are done concurrently. Hence, it is well adapted to parallel processing. The feature makes it more attractive for binary multiplications. This in turn reduces delay.

Divide the no. of bits in the inputs equally in two parts. Let's analyze 4x4 bit multiplication, say multiplicand $A=A_3A_2A_1A_0$ and multiplier $B=B_3B_2B_1B_0$. Following are the output line for the multiplication result, $S_7S_6S_5S_4S_3S_2S_1S_0$. Let's divide A and B into two parts, say "A3 A2" & "A1 A0" for A and "B3 B2" & "B1 B0" for B. Using the fundamental of Vedic multiplication, taking two bit at a time and using 2 bit multiplier block, we can have the following structure for 4x4 bit multiplication as shown in Figure.

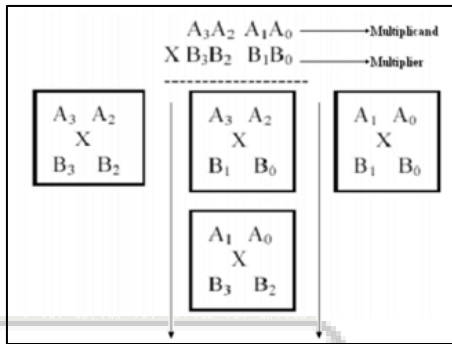


Fig. 4: Structure of 4x4 bit Multiplication

Each block as shown above is 2x2 bit multiplier. First 2x2 multiplier inputs are "A1 A0" and "B1 B0". The last block is 2x2 bit multiplier with inputs "A3 A2" and "B3 B2". The middle one shows two, 2x2 bit multiplier with inputs "A3A2" & "B1B0" and "A1A0" & "B3B2". So the final result of multiplication, which is of 8 bit, "S7S6S5S4S3S2S1S0".

To understand the concept, the block diagram of 4x4 bit Vedic multiplier is shown in Figure. To get final product $S_7S_6S_5S_4S_3S_2S_1S_0$ four, 2-bit Vedic multiplier and three 4-bit Ripple Carry (RC) Adders are required. In this proposal, the first 4-bit RC Adder is used to add two 4-bit operands obtained from cross multiplication of the two middle 2x2 multiplier modules. The second 4-bit RC Adder is used to add two 4-bit operands, i.e. concatenated 4-bit ("00" & most

significant two output bits of right hand most of 2x2 multiplier module as shown in Figure) and one 4-bit operand we get as the output sum of first RC Adder. Its carry "ca1" is forwarded to third RC Adder. Now the third 4-bit RC Adder is used to add two 4-bit operands, i.e. concatenated 4 - bit (carry ca1, "0" & most significant two output sum bits of 2 nd RC Adder as shown in Figure) and one 4-bit operand we get as the output sum of left hand most of 2x2 multiplier module.

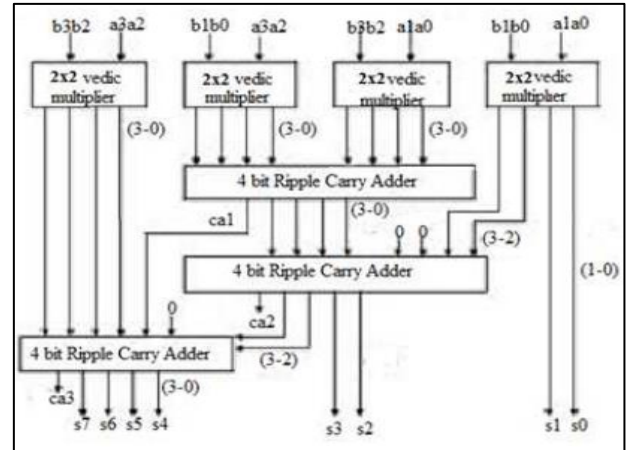


Fig. 5: 4X4 Vedic Multiplier

Early literature speaks about Vedic multipliers based on array multiplier structures. The arrangement of Ripple Carry Adder as shown in Figure helps us to reduce delay.

Bit Length	Type	Delay (ns)	Levels of Logic	No. of slice LUTs	Memory (KB)
2	Vedic	6.494	4	6	258052
	Array	6.494	4	6	258052
4	Vedic	7.942	5	7	255024
	Array	55.591	40	38	257284
8	Vedic	18.270	15	121	257988
	Array	120.485	175	82	259588
16	Vedic	27.278	23	656	259076
	Array	263.072	734	178	260868

Table 1: Comparison of Vedic and Array Multiplier

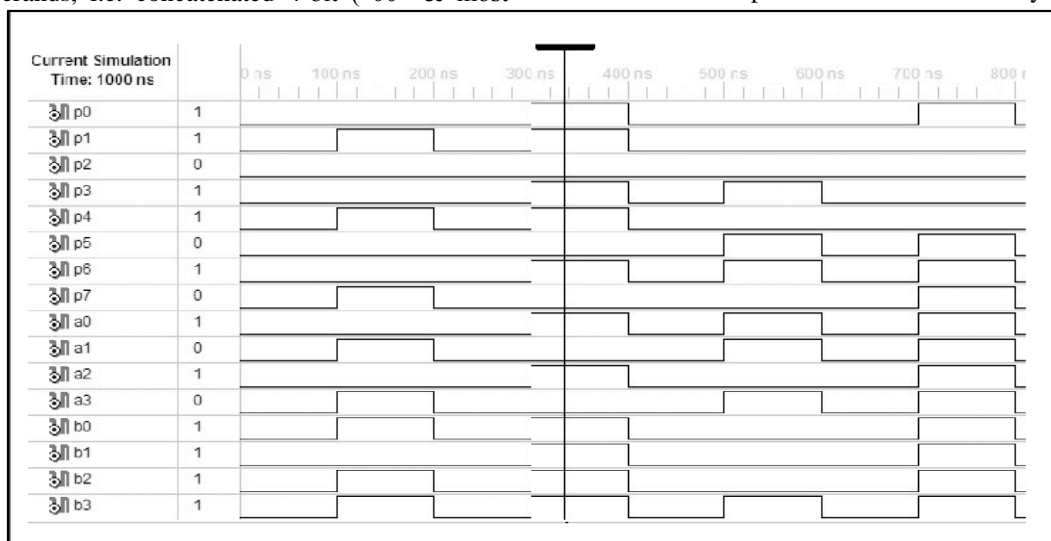


Fig. 6: Waveform for 4X4 vedic multiplier

VI. CONCLUSION

This paper represents the comparison between array multiplier design and 4 bit vedic multiplier with ripple carry adder using the UrdhvaTriyakbhyam sutra. The 4×4 Vedic multiplier is designed in T-spice, synthesized and simulated using Tanner EDA software and perform design rule. The simulation result shows that 4×4 Vedic Multiplier with Carry Look Ahead Adder is having less delay, low power consumption. In other words the Vedic multiplier has increase the speed of the processor and reduce the delay in various aspect.

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