

# Concatenated Code and MC DS CDMA Model in High Speed Vehicular Communication

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**Abstract**— Multi Carrier Direct Sequence Code Division Multiple Access (MC DS CDMA) technique is the future generation mobile communication system and to access technology in future advances. Serial and Parallel concatenated codes are used for correcting the errors in data transmission. We proposed hybrid concatenated code for MC DS CDMA structure and estimate parameters like memory and design time. Use of interleavers reduces the burst errors between outer and inner code of encoding and decoding operation in the MC DS CDMA model. Modelsim synthesis technology is used to simulate the entire model and Verilog Hardware Description Languages (HDL) is used for design the codes of MC DS CDMA systems and the computer simulations of FPGA Simulation demonstrate that the performance of the proposed scheme is investigated.

**Key words:** FPGA, MC DS CDMA, Modelsim synthesis, Serial and Parallel concatenated codes, Verilog HDL

## I. INTRODUCTION

The enormous growth of wireless mobile communication systems will be required to support high-speed transmission rate, high performance, high capacity and high bit rate. The main purpose of multiple access schemes is used to achieve number of goals such as to handle several numbers of users in the same channel without any mutual interference problem in it.

The MC-DS-CDMA technique is an important one for the Fourth generation (4G) system. Multi Carrier Direct Sequence Code Division Multiple Access (MC-DS-CDMA) has the highest degrees of freedom in the family of Code Division Multiple Access (CDMA) schemes that can be beneficially exploited during the system design and reconfiguration procedures. The design of low complexity rate compatible code and it provides both serial and parallel concatenated codes. Lower error floors and high code rates are obtained [5]. The serial to parallel converted data streams' using a given spreading code and then modulates a different subcarrier with each of the data stream. VHDL implementation of DS-CDMA transmitter and receiver has been proposed in this paper. Modelsim Xilinx tool will be used for functional simulation and logic verification at each block level and system level. The Xilinx Synthesis Technology (XST) of Xilinx ISE tool will be used for synthesis of transmitter and receiver on FPGAs.

In the recent years the CDMA on FPGA platform has attracted attention of academic research and industry. The Spartan TM-3E family of Field-Programmable Gate Arrays (FPGAs) is specifically broadband designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The five-member family offers densities ranging from 100,000 to 1.6 million system gates. Because of their exceptionally low cost, Spartan -3E FPGAs are ideally

suited to a wide range of consumer electronics applications, including access, home networking, display/projection, and digital television equipment. This Paper is organized as follows. The design of MC-DS-CDMA system and concatenated code are given in section II. In section III, the results are discussed. Section IV, Concludes the MC-DS-CDMA Communication system and concatenated code Model Design

## II. MC-DS-CDMA SYSTEM AND CONCATENATED CODE

### A. MC-DS-CDMA Communication System

CDMA is a channel access method used by various radio communication technologies. One of the basic concepts in data communication is the idea of allowing several transmitters to send information simultaneously over a single communication channel. CDMA allows Spread spectrum technique allowing multiple users to share the same frequency in one cell. It takes advantage of Multipath and Operates under presence of interference. MC-CDMA is a multiple access scheme used in OFDM-based telecommunication systems, allowing the system to support multiple users at the same time. MC-CDMA spreads each user symbol in the frequency domain. That is, each user symbol is carried over multiple parallel subcarriers, but it is phase shifted (typically 0 or 180 degrees) according to a code value. The code values differ per subcarrier and per user. The receiver combines all subcarrier signals, by weighing these to compensate varying signal strengths and undo the code shift. The receiver can separate signals of different users, because these have different (e.g. orthogonal) code values. One way of interpreting MC-CDMA is to regard it as a direct-sequence CDMA signal (DS-CDMA) which is transmitted after it has been fed through an inverse FFT (Fast Fourier Transform). Multi-Carrier Code Division Multiple Access (MC DS-CDMA) is a multiple access scheme used in OFDM-based telecommunication systems, allowing the system to support multiple users at the same time. Since each data symbol occupies a much wider bandwidth than the data rate (in bit/s). In the MC-DS-CDMA technique, the serial-to-parallel converted data stream is multiplied with the spreading sequence, and then the chips belonging to the same symbol modulate the same subcarrier. Here the spreading is done in the time domain. Thus this MC-DS-CDMA technique plays vital role in uplink transmission of wireless communication than any other access.

### B. Transmitter Model

The four user CDMA system consists of four mobile users who can transmit and receive data independently. For the transmission of data from four users over a common channel, four different 15 bit long mutually orthogonal spreading codes are used. The orthogonal spreading codes are generated

by using linear feedback shift register configuration. The entire LFSR is clocked simultaneously that produces a single bit shift along the entire register. The eight bit input data corresponding to a particular user is converted into serial form by an eight bit PISO. The PISO is clocked by  $F_{master}$  divided by 15 clocks where  $F_{master}$  is 0.5GHz. Then it is spreaded by the 15 bit PN code. The PN code generator is clocked by  $F_{master}$ . Spreaded data of all the four users are summed up and generated the signal to be transmitted.

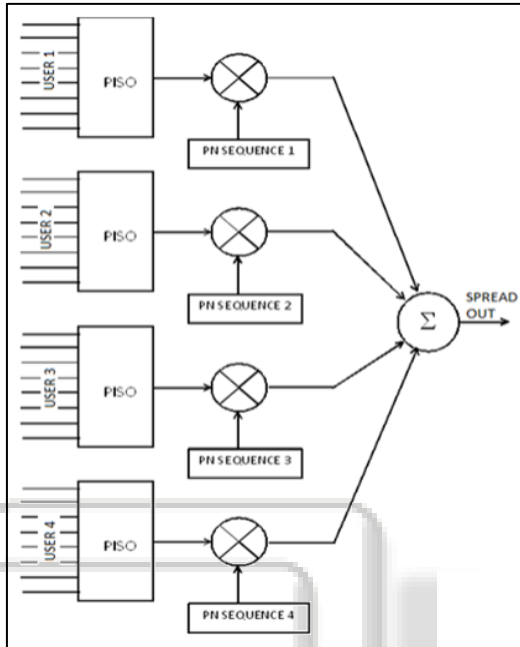


Fig. 1: MC-DS-CDMA Transmitter Model

C. Receiver Model

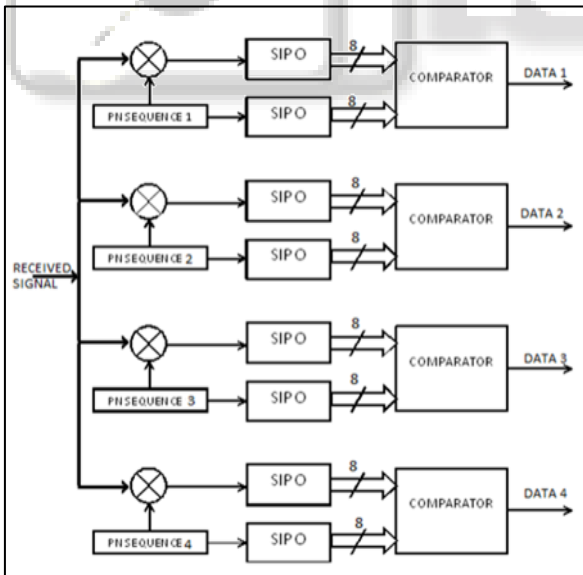


Fig. 2: MC-DS-CDMA Receiver Model

After de-spreading the received signal with the corresponding code, it is compared with the same PN code, which is converted into parallel, using an 8 bit comparator. The comparator uses 0.33GHz clock frequency. If the actual transmitted data was a high then the de spread output will be same as that of the PN sequence. So the comparison function is performed in such a way that, it compares the de spread output with PN sequence. If it is same, then it can be

concluded that the data send is a high and if it is not, then the data will be a low. So the comparator output corresponds to the actual transmitted data of a particular user. Thus it is able to reconstruct the original data from the spreaded output.

D. BPSK Modulator

The basic digital modulation scheme called BPSK and its performance in a Gaussian noise environment. The concept is simple. Whenever the transmitter wants to send a +1, it will transmit a positive co-sinusoid, whenever the transmitter wants to send a -1, it will transmit a negative co-sinusoid. If the transmitted information is 1, the modulated signal  $s+1(t)$  have a phase of 0. If the transmitted information is -1, then the modulated signal  $s-1(t)$  has a phase of  $\pi$ , or 180 degrees. Figure 4. Shows what the modulated signals look like in the time domain. The BPSK modulator is quite simple to implement. The modulator itself is no more than a multiplier. The input to the modulator consists of the data symbols. The data can be either a +1 or a -1. The data is multiplied by the Carrier  $\cos(2\pi ft)$  scaled by the coefficient  $\sqrt{2E/T}$ . The output of the multiplier is the corresponding modulated signal.

The noise  $n(t)$  is frequently modeled as an additive white Gaussian noise (AWGN) process.

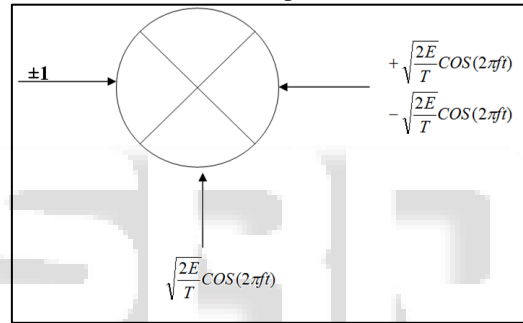


Fig. 4: BPSK Modulator

E. PN Sequence Generator

An ideal spreading sequence would be random sequences of binary ones and zeros. It is required that transmitter and receiver must have a predictable way of the random bits stream, at transmitter and receiver and yet retain the desirable properties of a random bit stream. The requirement is met by a PN generator. A PN generator will produce a periodic sequence that eventually repeats but in random manner. The code generator consists of essentially three elements – Delay elements, linear combining elements and feedback loop elements. The delay elements are connected in series. These elements are normally D-flip flops. Some of the outputs of the delay elements are combined in linear combining elements with the outputs of other delay elements and fed back to the input of the first delay element in the series. The implementation of PN sequence generator is usually made up of the linear feedback shift register.

F. Concatenated Code Model

Concatenating two convolutional codes in series gives serially concatenated convolutional codes (SC turbo codes). We arrive at turbo block codes by concatenating two block codes and at repeat-accumulate codes by concatenating a repetition code and a convolutional (accumulator) code.

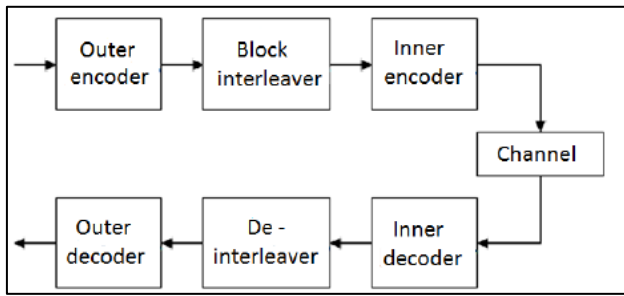


Fig. 3: Concatenated Code Model

The code rate of a systematic SC code with a rate  $r_1 = k_1/n_1$  inner code and a rate  $r_2 = k_2/n_2$  outer code is,

$$K/n = k_1/(k_1+n_2) = k_1/(k_1+n_1/r_2) = r_1 r_2 / (r_1 r_2 + 1) \quad (1.1)$$

From Equation (1), serial concatenation with a rate  $k_O/n_O$  outer convolutional code and rate  $k_I/n_I$  inner convolutional code, a fixed-length- $K$  message is encoded. The outer code can thus be considered as an  $(NO = Kn_O/k_O, KO = K, d_{min}(O))$  block code and the inner code as an  $(NI = KN_I/k_I, KI = NO, d_{min}(I))$  block code. Using a length  $NO = KI$  interleaver, the concatenated code is thus an  $(N = NI, K = KO, d_{min})$  block code.

### III. SIMULATION RESULTS AND DISCUSSIONS

The simulation of the designed components – MC DS CDMA, CDMA receiver, BPSK modulator, PN sequence Generator and Concatenated code model is obtained from XILINX.

The Figure 4 describes the device properties and the details of the FPGA used. The evaluation development board used is Spartan 3E – Starter board and the HDL language used is Verilog.

Property Name	Value
Evaluation Development Board	Spartan-3E Starter Board
Product Category	All
Family	Spartan3E
Device	XC3S500E
Package	FG320
Speed	-4
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	Verilog
Property Specification in Project File	Store all values
Manual Compile Order	<input type="checkbox"/>
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	<input type="checkbox"/>

Fig 4: Design Properties

Figure 5 and Figure 6 shows the RTL Schematic view of the MC DS CDMA Transmitter and Receiver respectively.

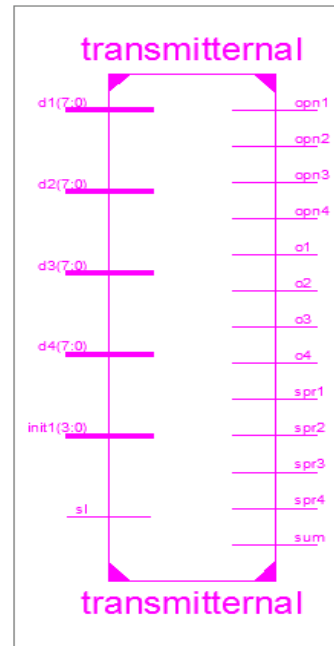


Fig. 5: RTL Schematic of Transmitter



Fig. 6: RTL Schematic of Receiver

The simulated waveforms of the final transmitter and receiver for 4 users are presented as follows.

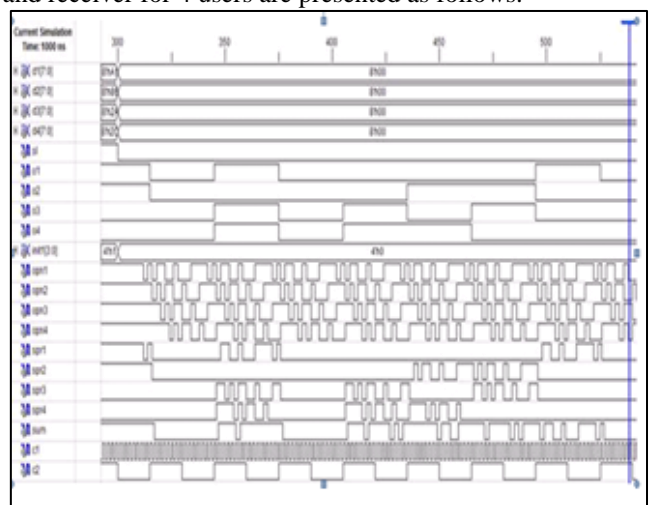


Fig. 7: Transmitter Output

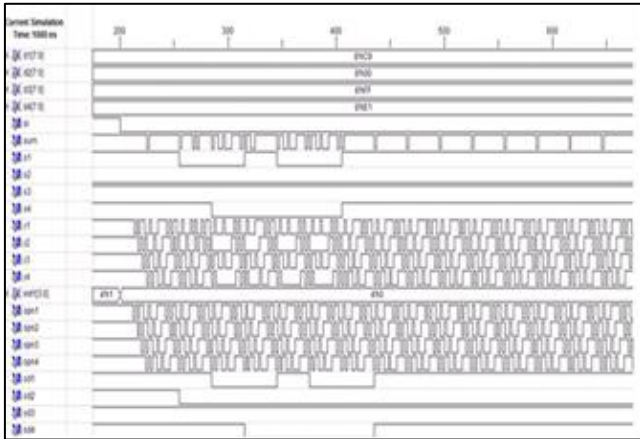


Fig. 8: Receiver Output

#### IV. CONCLUSION

The transmitter and receiver model for communication is implemented for MC-DS-CDMA Scheme. All components like transmitter, receiver, PN sequence generator, BPSK modulator were implemented using VHDL codes. The PN sequence is achieved by providing feedback from the outputs of some of the registers (called taps) according to minimal polynomial used. The feedback is then fed back into the most significant register after passing them through a modulo-2 adder circuit. The process of realizing LFSR is carried out by first developing the VHDL code for a D-flip flop. The same D-flip flop code is then called 4 times in the main VHDL program to realize the required LFSR. The VHDL code for implementing all subsystem circuits of transceiver are simulated on XILINX ISim and ModelSim and hence, the results were generated and tested successfully for a wide variety of message data selected randomly. Implementation was done using XILINX FPGA with clock frequency of 100 MHz range.

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