Design and Analysis of First in First out using Different Read and Write Logics in Verilog

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Abstract— FIFO is an approach for handling program work requests from queues or stacks so that the oldest request is handled first. In hardware, it is either an array of flops or read/write memory that stores data from one clock domain and on request supplies the same data to other clock domains following FIFO logic. Through analyzing on the FIFO module characteristics, we design and analyses FIFO using different read and write logics. We have considered 64 inputs, each having 32-bit data, and all of its feature implementations are described using Verilog HDL. At present, the scheme has been applied in the systems of distribution feeder automation, through detecting, which meets the system performance demands.

Key words: CPLD; FIFO; FTU; Data Cache; Real-Time Monitoring

I. INTRODUCTION

This article is mainly about Feeder Terminal Unit research, FTU is a main device in Feeder automatization system, which is used to real-time monitor the pole top switch and finish remote control and detection capabilities, providing distribution system of the operation and the various data , implementation of the order which released from main station[1], monitor and control to power distribution equipment ,to complete fast recovery to fault defined, fault isolation zone and non-fault isolation zone, real time supply of data is crucial to the data and processing data is very large, the existing solutions, usually adopted Digital Signal Processor DSP, and EMAC controller first input and first output FIFO.

But it is not enough to support the system of data is stored temporarily, FTU is difficult to satisfy the timely request, to achieve the goal, we need big capacity and high speed of data cache, and the bulk of rapid FIFO chip is not only expensive, but also limited for use in practical applications, so looking for bulk, fast, cheap, flexible FIFO was necessary. ALTERA provide complex programmable logic device, component CPLD, EPM3256AS resolve the conflict, it is not only flexible, high speed ,big capacity and high reliability, and its high levels of integration and use broadly, powerful functions[2,8], you can hardly needs any functional hardware module to meet the required functions of FTU. So this article applies for EPM3256AS to build up data buffer and use for FTU.

II. FIFO INTRODUCTION

FIFO is the device of First Input First Output, the first to enter the data will be the first to be removed. The difference with ordinary memory is without external read and writes the address, the data read and write the address

Byautomaticallyadd1.Forprocessingandtransmissio nof data flow, match the data transmission of different clock domain and width of the data interface, in order to improve the system performance. Figure1isthebasicprincipleofa model chart FIFO.

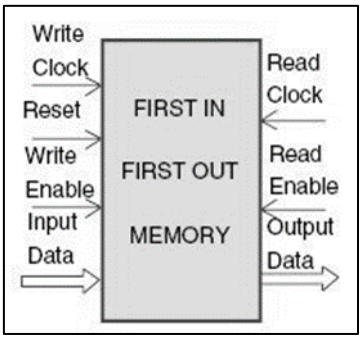

Fig. 1: FIFO model

The principle that reset for FIFO RST first; Then CLR clears to zero. If CUP1 write FIFO data, the first detected with a full mark. If Full sets 0, FIFO is full; If Full sets 1, you can input data to FIFO. If CUP2 is reading data from FIFO, then first inspection to empty, if Empty sets0, FIFO is Empty; If Empty sets 1, you can read data from FIFO, data is Sequential write, and sequential read.

III. SYSTEM HARDWARE ELECTRICAL ROUTE DESIGN

A. System general hardware structure

In system design for hardware, FTU will be divided into four pieces, one is PTCT; a piece of the master with eight road of simulated switch; a piece of the MCU, including DSP CPLD, A/ D converters, the expansion or enlargement SRAM and FLASH,RTL8019 Ethernet controller, output coupler group relay group consisting of such data, signals, other modules; there is a block of input and output, including CAN bus driver, RS232/485; Such design and structure of FTU is level modular, stability and interference immunity ,and the convenient and simplified system adjusting work.. Figure 2 shows the present system hardware structure chart.

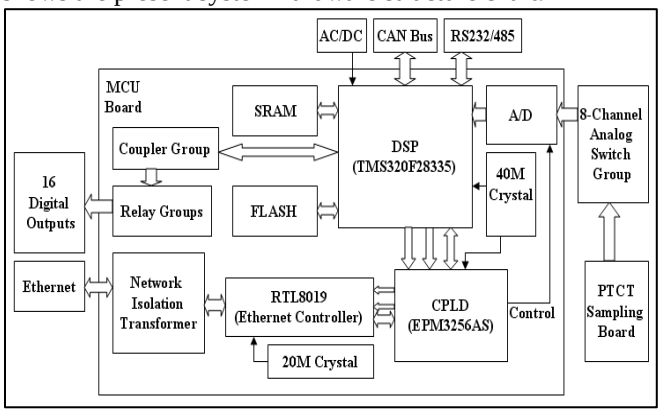

Fig. 2: System general hardware Structure

B. Network communication electrical module design

1) Hardware Selection

We use DSP, CPLD, RTL8019 Ethernet controller and network isolation transformer.

DSP use TMS320F28335 of 32bit from TI, it is a floating-point of DSP controller, 150MHZ frequency and large of precision and data processing capability CPLD use EPM3256AS of ALTERA Company. It is a high performance and low cost logic device made with CMOS EEPROM process, including 256 macro cells, operating voltage 3.3V, each I/O pin scan be fully accepted 5.0V, 3.3V, 2.5V, compatible with the IEEE1149.1-1990 (JTAG) standard test stimulus side and boundary scan capabilities [6], which uses a continuous connection structure and is easy to predict the delay, that makes the circuit simulation more accurate [4,5].

Ethernet controller us eRTL8019madebyTaiwanchip manufacturers REALTEK company, which supports multiple types of embedded chips and meets Ethernet II and IEEE802.3 standards(10base5, 10base2 10boseT), and with full-duplex communication interface, that is an ideal device for Ethernet communications[3].

Network isolation transformer has two major effects. One is the transmission of data and two is segregated network by a different device with difference from electrical level, in order to prevent of destroy the equipment with different signals transmitted by the voltage net line. In addition, Network isolation transformer can play a role preventing lightning and anti-electromagnetic interference for FTU.

2) Network Data Process Analyses

Ethernet interfaces over the internet network data from which a signal voltage transformer and smooth, and then get RTL8019 Ethernet controller, when RTL8019detected on a data, the CPLD, "to achieve the CPLD FIFO data cache, we can control RTL8019 can be cached the data, through the CPLD makes the system resets which can recognize the default RTL8019 way (PNP); only when FIFOfullmarksfor1,FIFOnullflagsfor1,thentheFIFO can get into the network of communication, then it can be written or read FIFO cache unit. It is a l so important to note that each CPLD to send or receive RTL 8019 DSP from the interruption, to make the modules clear to zero. Otherwise, the CPLD will not respond to or in response to the next break. At last the DSP reading from CPLD and cope with it.

IV. FIFO DESIGN & ACHIEVE

A. FIFO top level module logic principle design

The CPLD use modular design, the basic data of designing FIFO recovery is 16-bit data width,8-bit data depth, two internal guideline (which based on actual application needs to make changes). The internal logic of CPLD contains dual-port RAM controller module, buffers, controller module and monitor module, as shown in Figure 3.

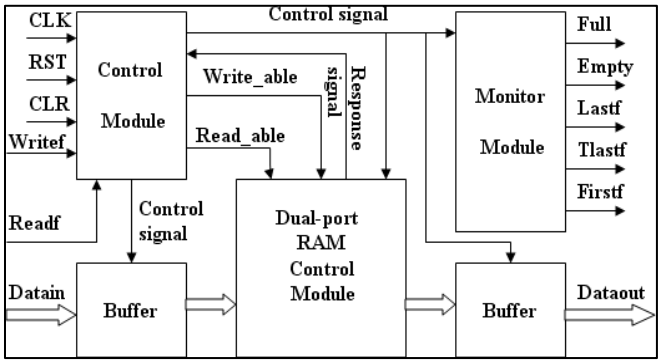

Fig. 3. FIFO module based on the logical structure of CPLD

B. FIFO every level module logic principle design and Achieve

For the design and implementation of control module: one is logical device RST reset and CLR to zero, and to monitor the module and a corresponding buffer control signals, dual-port RAM control module will respond signals; the two was in its internal there are two main parts, they were written control logic module and logical control, is primarily used to produce FIFO state of the enormous able to write, write to read, and enormous able to control buffer to dual-port RAM module, or read data from dual- port RAM.

The design and implementation of the modules: in its interior has a key module, it is free and full of a logic, in the network data transmission, if the operation to the port of the RAM module of the data and FIFO in full, FIFO monitor module send a full marks and to stop writing action continued to write data in a FIFO; FIFO monitor module sent a mark empty signal to prevent the reading action continued reading data. the invalid data signal indicates FIFO lastf in a space can be put on a data signal; t lastf value of a signal that FIFO has space to put in two data value of a signal; firstf FIFO that one valued signal .For the implementation of buffer in the power system, the data is large for FTU and the main station, network data bus is in rather than concurrently, the equipment of interaction between the speed is very strict (real-time monitoring and needed in dealing with problems).Each device for 5ms transport 5K-10K, Ethernet per second produced the size of data about 1MB – 2MB, a group of line is twenty equipment, a device is a need to accept most of the 40MB. In addition, because the CPLD RTL8019 writing and reading out data speed is low, nearly 20mhz, which the CPLD out connection CLK is 40MHZ, this is different world, so need buffer as input and output cache, used to temporarily store data, network of coordination and buffer, the realization of network data transmission.

Dual-port RAM controller module structure is shown in Figure 4, which includes initialization module and read/write control module, dual-port RAM. The key of the design of the controller module is read/write timing.

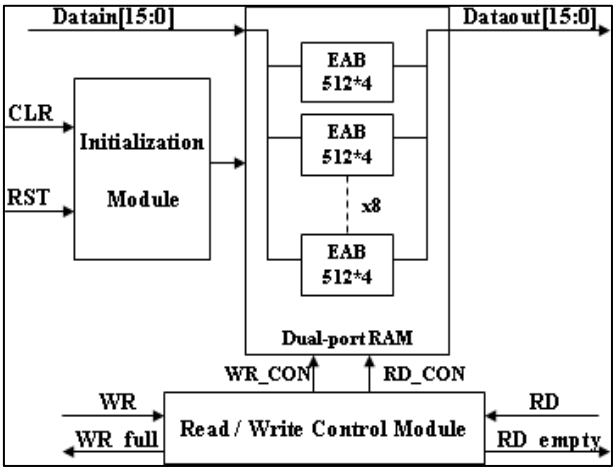

Fig. 4: Dual-port RAM controller module structure

Initialization module mainly initializes dual-port RAM. After the electricity and time signal is stable, the signal to CLR to zero waiting for the signal 50ms RST clear signal, waiting for 30ms, and against all logic devices that perform operations, all logic devices in a free state. For dual-port RAM for real-time data cache, it can improve throughput of FIFO. For the depth (capacity) of FIFO, eight EAB of 4-bit 512k are used in the figure. Read and write control module is a double port control module RAM of the principal control module and its internal to produce two control signals; one is the WR_CON write control signals, RD_CON read control signal. when the written over, signal control module began to read and write to the port of the RAM module, it shows it can write data, if it detects the data is full, on the external control module sends WR_full marks with the signal; When rd read transfer, read and write control module began to send RD_CON to RAM, that shows we can read the data, if it detects that data was empty, to sends an RD_empty control signal to external control module. In addition, read/write control module has an important role to be coordinated between timing relationships of the modules, to meet dual-port RAM read / write timing requirements necessary to, dual-ports have to determine the status of the RAM to read and write.

V. EMULATION

The design is completely described using Verilog HDL language. The achieved FIFO sets the clock input clk, reset input rst, clear input fclrn, read and write signal input f out n and finn, parallel data input and output data in and data out,full marks full, empty flag empty n, a data value of the register state output Lastf in the space, two data value of the register state output T lastf in the space, and one only data value of the register state output Firstf in the space.

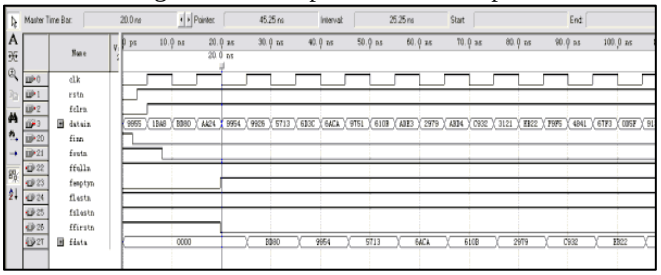

Fig. 5: Simulation output

Simulation of the FIFO module uses Platform with Quartus II8.0. As shown in Figure 5, time interval is set to 1 ms.Clk time reset settings for 10ns rstn 3ns after a "1", fclrn 5ns to zero after the "1", 16 data transmissions the width. The internal guide line safter the count are cleared to zero, ffulln sign a "1", femptyn is "1" after 20 ns, finn is "0" after 2ns, foutn is "0" after 8ns. We set a group of random data (16 hex) in the datain signal line, and receive the random data where corresponds to the read pulse in dataout signal line.

Simulations indicated that the implementation of processes is accurate. FIFO use the software to create and configure file download epm3256as by cable to chip in the tests conducted by the hardware and normal. The number of macro-cells which the achieved FIFO requires is 93, only 36% of overall resources.

VI. CONCLUSION

The design has been applied to data cache in real-time monitoring and rapid trouble shooting system. CPLD device is used to achieve FIFO data cache. First it is not only greatly simplify the structure of the printing system ,to reduce the area of the system has a low consume, high stability and high reliability, high efficient and universality, flexibility, but also shorten the period of system development, convenient system debug and maintain; Second the requirement of 5K-10K data amount between each device within 5ms is achieved to make the FTU real-time monitoring, fast processing capability improved greatly, to satisfied with the network feeders automated system applications. Therefore, study has a very important practical significance on using CPLD devices to achieve FIFO data buffer.

VII. REFERENCES

[1] Tao Weiqing,Wang jun.TMS320F2812-101 protocol-based implementations in the FTU[J]. Electronic technology, Aug, 2007:pp1-2.
[2] Liu Caixia, He Zhanchuang.CPLD-based parallel data collection and storage [J]. Modern electronic technology, Sep.2008, (5):pp84- 86.
[3] Liu Haibo,LiuRuiyu,Zheng Guilin. The Preparation of the Underlying NIC Driver [J]. Modern computers (Professional Edition).22.May.2009 (6):pp90-92.
[4] Chen Zhongping,GaoJinding,GaoJianfang. Quartus II on the CPLD / FPGA design and practice [M]. Beijing: Electronic IndustryPress.2009:pp3-44.
[5] Samir Palnitkar. Verilog HDL A Guide to Digital Design and Synthesis Second Edition [M]. Beijing: Electronic Industry Press.NOV.2004:pp40-111.
[6] HouBoting, GuXin. VHDL Hardware Description Language and Digital Logic Circuit Design [M].xi'an: Xidian University Press.2009:pp22-28.

