Zipper Circuit for Low Power and High Speed Applications in VLSI Design

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Abstract— A low power low cost CMOS NP Domino logic is design. The NP Domino logic designs require fewer transistors and are compatible with full Domino logic. The performance of NP Domino logic is also better compared to the standard Domino logic implementations. Dynamic domino logic are very good but had many challenges like monotonicity, leakage, charge sharing and noise problems. These problems are totally eliminated in the CMOS NP Domino logic which is also known as Zipper circuits without any penalty in performance or silicon area utilization. This paper compares NP Domino logic with static CMOS and domino logic design implementations.

Key words: Zipper, CMOS, NP Domino Logic, Monotonicity

I. INTRODUCTION

Dynamic CMOS circuits had better performance and require less silicon area than conventional static CMOS circuits. There are various dynamic schemes that had been proposed, Domino CMOS, NORA CMOS

Pipelined logic structures etc. [1] [2]. All these design styles employs a single phase clock to drive their circuit's gates, exploiting the full inherent speed of the dynamic gates. The dynamic stage of all Domino CMOS is composed of N logic and eliminates the internal race conditions by using a buffer at the output of every stage that produces only noninverting signal. This problem is solved in NP Domino (Zipper or NORA) [3] circuits

Which employ a pipelined structure of NP CMOS and clocked CMOS latches. Since NP Domino circuit has no inverter at the output of each stage, it is generally composed of fewer transistors than Domino CMOS circuits. It also offers more logical flexibility by providing both inverting and noninverting signals at the output. The dynamic Domino CMOS circuits also suffer from signal degradation caused by leakage current and charge redistribution. Many alternative solutions like complex clocking, extra transistors or large buffer [2] have been proposed to solve these problems. In this paper, we introduce a CMOS that incorporates all the advantages of Domino CMOS. NP Domino CMOS are immune to the problems of instability and charge-sharing. The area utilization is also better than the Domino CMOS. In the section that follows, we will describe the dynamic CMOS structure and its features and later deal with the performance of NP Domino CMOS logic circuits [4].

II. DIGITAL LOGIC STYLES.

The cascading of dynamic logic from one gate to other gives problem. The precharge "1" state of the first gate causes the second gate to discharge prematurely, before the first gate has reached its correct state as shown in Fig. 3. This uses up the "precharge" of the second gate, which cannot be restored until the next clock cycle, thus there is no recovery from this error. The solution to cascade dynamic logic gates is Domino Logic

that inserts an ordinary static inverter between the two stages. Although the inverter has a pMOS (one of the main goals of Dynamic Logic is to avoid pMOS where possible, due to speed), there are two reasons it works well. First, there is no fanout to multiple pMOS; the dynamic gate connects to only one inverter, so the gate is still very fast. Furthermore, since the inverter connects to only nMOS in dynamic logic gates, it too is very fast.

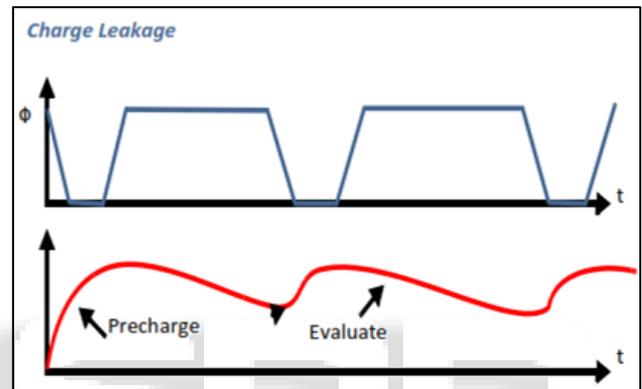Secondly in some types of logic gate the pMOS in an inverter can be made smaller.

Fig. 1: Charge Leakage waveform

III. DOMINO CMOS CIRCUIT

Cascading of Domino logic produces ripples to every evaluation stage of the cascaded structure, similar to a domino falling one after the other. Once fallen, the node states cannot return to "1" until the next clock cycle, justifying the name Domino CMOS Logic. It contrasts with other solutions to the cascade problem in which cascading is interrupted by clocks or other means. They have smaller area than the conventional CMOS logic. Higher operating speed is possible as their parasitic capacitance is less and operation is free of glitches. In Domino CMOS charge distribution may be a problem and only non-inverting structure are possible. The precharge and evaluate condition are as follows:

A. Precharge condition:

When φ=0, the output node Out is precharged to VDD by Mp.

B. Evaluation condition:

When φ=1, me is on and node Out discharges conditionally, depending on the value of the input signals.

During evaluate if no path exists, then out remains high via CL (diffusion, wiring and gate capacitance). Once Out is discharged, it cannot be recharged. Therefore, the inputs can make at most one transition during evaluation. The Domino logics are characterized as

C. Properties:

a. The logic function is implemented in the NMOS pull-down network. b. The number of transistors is N+2 instead of 2N c. It is non-ratioed (noise margin does not depend on transistor ratios). d. It only consumes dynamic power. e. Faster switching due to reduce internal and down steam capacitance. The basic diagram for Domino CMOS are shown in Fig. 5
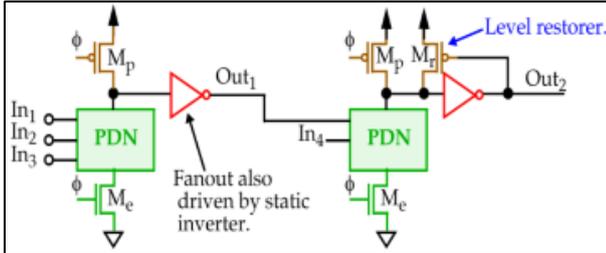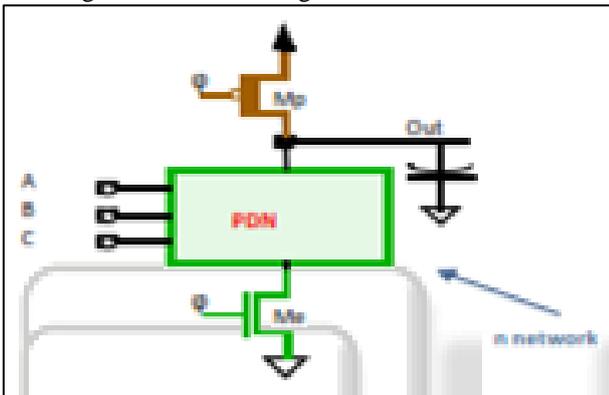
Fig. 2 Basic Block diagram of Domino CMOS
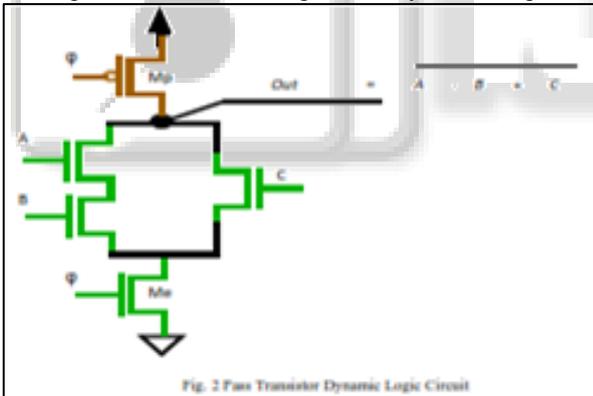
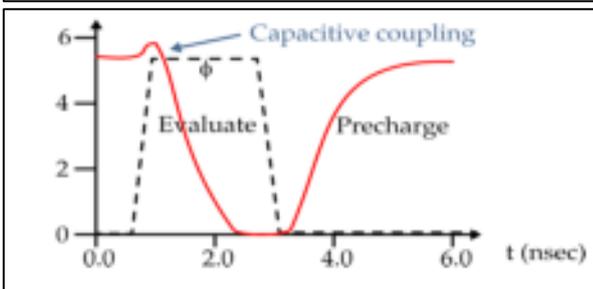Fig. 3: Basic Block Diagram of Dynamic Logic

Fig. 4: Precharge and evaluate wave form
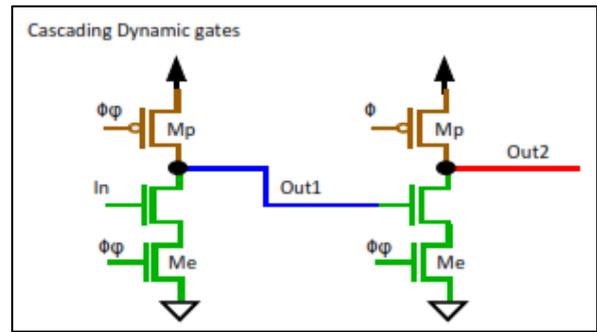
Cascading Dynamic gates

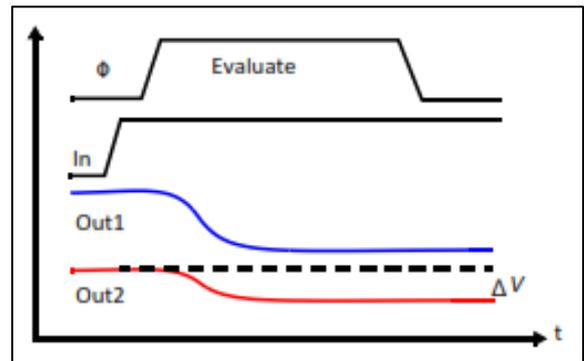Fig. 5: Domino CMOS (MOS Level)

Fig. 6: Precharge and evaluate waveform

IV. NP DOMINO CMOS CIRCUITS

NP Domino CMOS, called as Zipper [2] logic is shown in Fig. 8. It has two major components: the Zipper Driver and alternate N and P dynamic logic blocks. The Zipper Driver is controlled by a single phase clock that generates strobe signals, which drive all subsequent N-P blocks. During precharge, every output of N block is high and every P block is low. During evaluation, each output of N stage will undergo only one transition from high to low and the output of each stage will undergo only one transition from low to high. This "staggered" fashion in which signals propagate down each stage of the circuit gives rise to the name "Zipper CMOS". The major problem of NP Domino logic circuit is the internal nodes which may share charge with the output node, resulting in false output values in certain situations. The problem can be solved by either inserting extra transistors within each N block and P block that sustain the precharged value of the internal nodes or supply separate clocks to precharge transistor and the access transistor. The better solution is to supply separate clocks to the precharge transistor and the access transistor.

The main purpose of the Low Voltage [5] logic style is to increase the current level for low supply voltages without increasing the transistor widths. The High speed and Low Voltage domino inverter is shown in Fig. 9. The clock signals φ switches from 1 to 0, the circuit is in precharge/recharge phase. During the precharge phase, RP1 turns on and recharges the gate of EN1 to 1. Meanwhile φ switches from 0 to 1 which turns on RN1 and recharges the gate of pMOS transistor P1 to 0. Thus both EN1 and P1 turn on in the precharge phase and precharge the output node Vout to Vdd. Fig. 9a describe the precharge mode of this circuit. In the evaluation phase, clock signals φ and φ switch from 0 to 1 and 1 to 0 respectively. Both recharge transistors RP1 and

RN1 switch off which make the charge on nodes Vp and Vn to be floating shown in Fig. 9b. The output node Vout floats as well until we get a transition on the input node. The input signal Vin must be monotonically rising to ensure the correct operation for the N type domino inverter. This can only be satisfied if a) input signal Vin is low at the beginning of the evaluation phase, and b) Vin only makes a single transition from 0 to 1

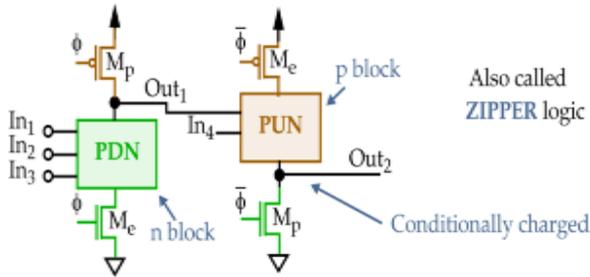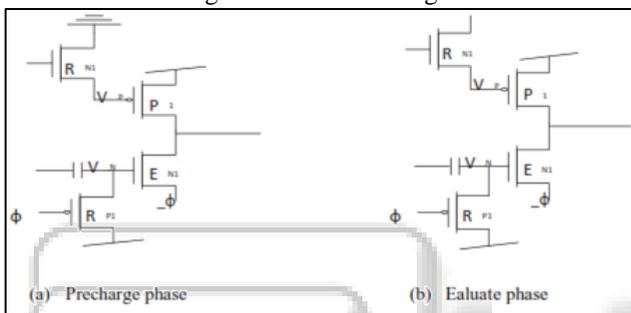Fig. 7: NP Domino Logic

Fig. 8: NP Domino Inveter: a) Precharge Phase b) Evalute Phase

V. SCHEMATIC DESIGNS

Different logics of the NP domino inverter are possible. The inverters can be used to implement AND2 and NAND2 functions by using one of the inputs to set the precharge level. The delay of the gates is dependent on the input delay. The delay of the AND2 and NAND2 gates are less than 10% of a standard complementary inverter for supply voltages 400mV. The typical delay for a NAND2 ULV gate is less than 10% of a CMOS inverter and the delay variation is also significantly less than for complementary CMOS. The delay variation is proportional to the delay, i.e. current level.
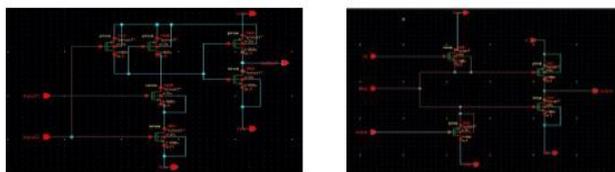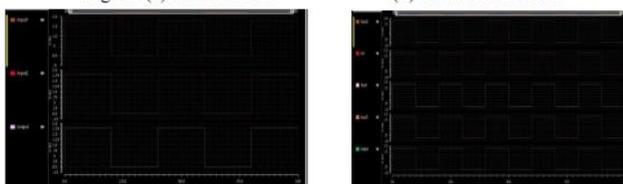

Fig. 10 (a) CMOS AND   (b) NP Domino AND

Fig. 11 (a) CMOS AND I/O waveform   (b) NP Domino AND I/O waveform

VI. CONCLUSION

Different low-voltage NP domino logic has been presented in this paper. The low voltage domino gates logic are high speed, i.e. the delay compared to a static CMOS logic is less than 5% for a supply voltage equal to 320mV. The energy delay product of the proposed low voltage PN Domino is less than 1% relative to the static CMOS logic when the circuits operate at a supply voltage below the threshold voltage of the transistors. The low voltage Domino can be used to design high speed and low voltage Full adders without applying parallel design which reduces both the power and the area.

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