A Review on High Speed CRC Encoder & Decoder based on FPGA

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Abstract— Cyclic redundancy check (CRC) technique is one of the most efficient error detection method, which used to detect single and burst errors. CRC method adds redundancy bits to the original data. The reminder of division between original message and selected polynomial is represents redundancy bit. At the receiver side, the received data can be recognized as valid or not. Generally speaking, (CRCs) are used to detect errors from noise in digital data transmission. The technique is also sometimes applied to data storage devices, such as a disk drive. They also have been turned to verify the integrity of files in a system in order to prevent tampering and suggested as a possible algorithm for manipulation detection codes .A Cyclic Redundancy Check (CRC) is the remainder or residue of binary division of a potentially long message, by a CRC polynomial. Per packet operation is necessary for IP protocol, design a new efficient technique using FPGA in case of CRC .This approach is memory efficient and operate at high speed, since most of method currently employed based on look up table consume more time ,more space and also there will be a ROM which stores the look up table. This paper presents high speed CRC encoder and decoder using FIELD PROGRAMMABLE GATE ARRAY, to increase throughput pipeline method is used.

Key words: Cyclic Redundancy Check (CRC), Encoder, Decoder, Field Programmable Gate Array (FPGA), Serial CRC, Parallel CRC

I. INTRODUCTION

The need of a communication system depends on how it deals with the noise that may interfere with the data to be transmitted. Optical fibers, transmission lines, air, space etc. are the medium of communication which can be affected by error. The coding theory is an important tool for encrypting a given message, decrypting and correcting the received message. Cyclic codes are one of important tool which used for encoding and decoding of the information represented in the form of binary numbers. .cyclic Codes were first implemented in 1957 by Prange. After that they became an essential part of coding theory. Cyclic codes are easy to study and implement because: Encoding and syndrome computation process can be perform easily. Because of elementary algebraic structure they are easy to decode. CRC is a type of important linear block code, which has the advantages of simple coding and decoding as well as strong capacity of checking errors and correcting errors. Therefore, it was mostly used in the field of communications and industrial measurement and control system whose industrial environment was even not good. The evolving world of telecommunications needs high reliability and improved speed in communications. Reliability in information storage and transmission is provided by coding techniques. Information is generally coded in bit streams and transmitted over the communication medium, channel. Because of a noise present in the analog part of the channel communication network tends to error. Therefore errors should be detected and corrected in decoding process. CRC is an error-detecting code designed to detect sudden changes to computer data, and mostly used in digital networks and storage devices example is hard disk drives. Blocks of data entering these systems get a short check value attached, derived from the remainder of a polynomial division of their contents. CRC is an error detecting code that is widely used to detect corruption in blocks of data that have been transmitted or stored. The basic idea of CRC is binary division which is different from other error detection method which is based on parity check. The CRC depends on reminder of division at transmitter i.e. encoder which it is added to original data and transmitted. There are two main point of CRC should be taken in the hardware design .The initial stage is reminder and redundancy zero at encoder side is equal to each other, and also less than the divisor bits by one bit. Second important stage is that the received data is divided by the same divisor which used at transmitter section. At the receiver section i.e. The generator polynomial divide the incoming information bits at the receiver section, then the reminder of division is lead to knowing if data unit is correct or corrupted if the string of bits arrives without error, the CRC decoder checkers get a zero reminder, if it has been corrupted during transmission the division reminder is not equal to zero. Two main types of CRC's are Serial CRC generator and Parallel CRC generator usually, the hardware implementation of CRC computations is based on the linear feedback shift registers, which handle the data in a serial form. Stills, the serial calculation of the CRC codes are unable to give a high throughput. Hence, to overcome that drawback we can use Parallel CRC generation.

A. Serial CRC Generation

Here CRC process is perform serially. The data input will be single binary and each clock pulse the data input will be one. There will some delay present between the consecutive data inputs and the output will be zero if the data will be encoded with same CRC value otherwise it shows non-zero value. The data is serially processed; the polynomial is XOR with the data input, that will be given to the D flip-flop (output same as the input) final CRC is generated as serially.

B. Parallel CRC Generation

Every modern communication protocol uses one or more error-detection algorithms. CRC is by far the most popular. CRC properties are interpreted by the generator polynomial length and coefficients. The protocol specification usually explains CRC in hex or polynomial notation. Parallel CRC calculation can significantly increases the throughput of CRC calculation.

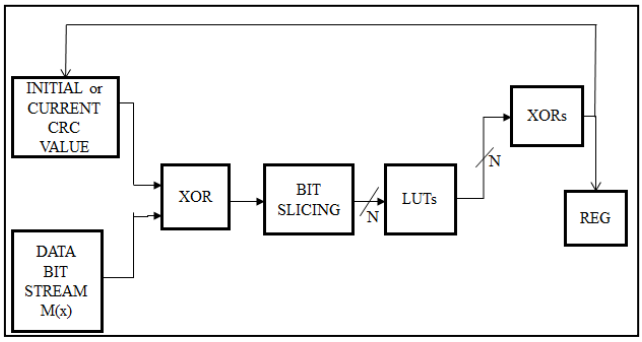


Fig. 1: Shows basic Operation of CRC Generator

II. LITERATURE REVIEW

X.-H. Peng and P. G. Farrell [1] proposed Golay codes are error detection and correction codes and it corrects errors in the receiving end in the received data to reduce retransmission events. Encoding algorithm for both the binary Golay code (G23) and extended binary Golay code (G24) implementation based on cyclic redundancy check encoding method. Decoding architecture for G24 (24, 12, 8) based on an error detection and correction method and here correction upto four erros is possible in the data. Synthesis and Simulation results obtained in Xilinx tool. Debugging FPGA design using XILINX Chipscope Pro tool.

Constantin Anton, Laurentiu Ionescu, *Ion Tutanescu, Alin Mazare, Gheorghe Serban [2] presented an efficient algorithm for parallel computation of the CRC in data transmission. Using CRC style checksums (cyclic redundancy check) is a simple and powerful method for detecting transmission error in data communication system. It is well suited for high speed serial transmission equipment, because it can be implemented on chip with a shift register and same XOR gates at nearly no cost. However, for some purposes it is necessary to implement a CRC calculation of the serial transmission chip, e.g., in additional error detection isrequired. The hardware implementation has been usedto improve the computation speed.

Gaurav Chawla and Vishal Chaudhary [3] presented a technique which states the message bits were encoded and decoded both on software and hardware environments. The error bits were detected and successfully corrected both on hardware and software platforms. The VHDL design core both for Encoder and Decoder can be used to program the FPGA chips in accordance to the need in various applications.

Payal.S.Hajare, Kanchan Mankar [4] praposed a technique of Design and Implementation of Parallel CRC Generation for High Speed Application. Parallel implementation is adopted which does not takes much time. CRC gives trade of between flexibility, performance and cost has been taken further than those enabled by tradition heterogeneous architectures based on microprocessor, DSP. CRC is very useful for error detection during data transmission. Having a look on the "CRC error detection method", we can prefer that the method identifies the error correctly. Thus the „Parallel CRC generation and checking" is more efficient than the „Serial CRC generation", it gives us the efficient result.

Hitesh H. Mathukiya and Naresh M. patel [5] proposed A Novel Approach for Parallel CRC generation for high speed application which states that high speed data transmission is the current scenario in networking environment. With challenging the speed of transmitting data, to synchronize with speed, it's necessary to increase speed of CRC generation. Starting from the serial architecture identified a recursive formula from which parallel design is derived. This paper presents 64 bits parallel CRC architecture based on F matrix with order of generator polynomial is 32. Proposed design is hardware efficient and required 50% less cycles to generate CRC with same order of generator polynomial. The whole design is functionally verified usin Xilinx ISE Simulator..

G.Shanthi, Dr.K.Srivas RAO ,,S.Srilekha [6] proposed a method This brief lays out FPGA implementation of encoder and decoder for Golay codes. Golay codes are error detection and correction codes and it corrects errors in the receiving end in the received data to reduce retransmission events. Encoding algorithm for both the binary Golay code (G23) and extended binary Golay code (G24) implementation based on cyclic redundancy check encoding method. Decoding architecture for G24 (24, 12, 8) based on an error detection and correction method and here correction upto four erros is possible in the data. Synthesis and Simulation results obtained in Xilinx.

Md Farukh Hashmi, Avinash G. Keskar [7] proposed a method of An Optimized which states that a Technique to model the error detection circuitry of CAN protocol in VHDL is described. The referred paper describes error circuitry in case of 'no error' our contribution – after reviewing the paper we designed error controlling circuitry for CAN bus in case of error.

III. PROPOSED WORK

Other error detection methods which is based on parity check is totally different from CRC. The CRC depends on reminder of division at transmitter i.e. CRC encoder which it is added to original data and transmitted. There are two main point of CRC should be taken in the hardware design .the initial important stage is reminder and redundancy zero at encoder is equal to each other, and less than the divisor bits by one bits .The next one is that the received data is divided by the same divisor which used at transmitter. At the receiver CRC decoder the incoming information bits is divided by the generator polynomial, then the reminder of division is lead to knowing if data unit is correct or corrupted if the string of bits arrives without error, the CRC decoder checkers get a zero reminder, if it has been corrupted during transmission the division reminder is not equal to zero .In this paper CRC encoder and decoder circuit is designed with divisor polynomial X+X+X+1 which is used at Asynchronous transfer mode(ATM) headers .ATM header is a type of a synchronization using in ATM protocol and other similar protocols. The CRC based framing was developed to improve the efficiency of pre standard (ATM) protocol link. This methodology is used in the ATM protocol link. The CRC method based framing reusing the header (CRC), which is present in ATM and other similar protocols to provide framing with no overhead adding on the link. So to design CRC encoder random input data supposed and sequence

procedure is explained as shown in fig. The basic block diagram of CRC encoder is shown in fig2.

According to CRC process a specific polynomial has to be chosen which called as divisor polynomial. The message is called as dividend, and to divide message divisor polynomial is used which generate reminder of equation. Module-2 division method is used for this operation, carry bit and borrow bit are generated in addition and subtraction method simple XOR is perform when it necessary. The message appended by number of 0's less than number of bits have to be transmitted. Then further division is applied which generate reminder. Reminder is then replace by zeroes at the end of message sequence and then transmitted. On the receiver side a data- word are received which contain data-bit appended with the reminder. To generate another reminder data-word is divided by same generated polynomial. If at output of polynomial is 0 then data received error free, otherwise received message consider as error message. This whole process is called as CRC technique.

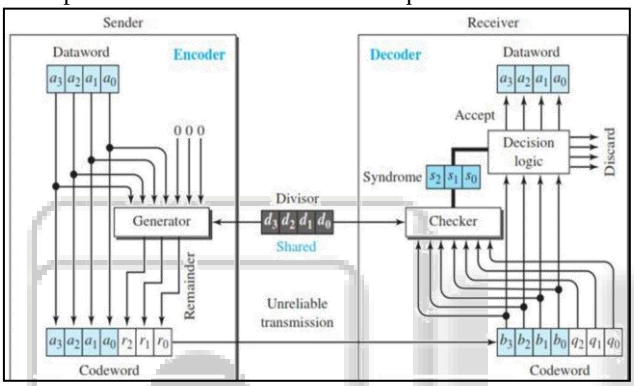
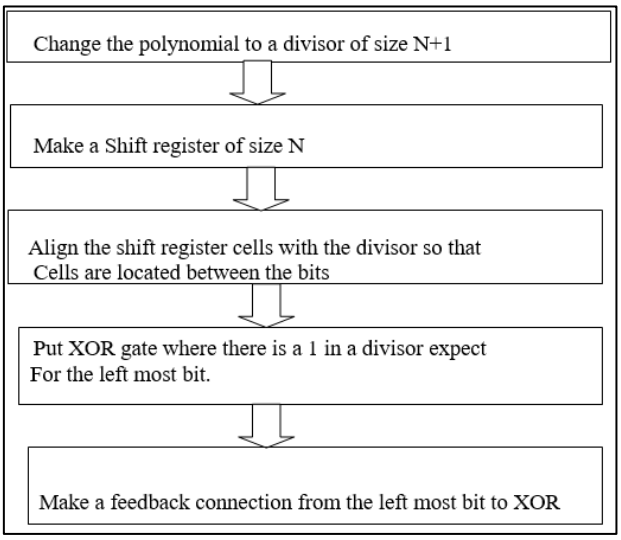


Fig. 2: Basic block Diagram of CRC Encoder and Decoder

Pipeline method: In computing, a pipeline is a set of data processing element connected in series, where the output of one element is the input of the next one. The elements of a pipeline are often executed in parallel or in time sliced fashion are to assembly line. Pipelining doesn't decrease the time for processing a single datum. "High" pipelining leads to increase of latency pipe .A pipelined system typically requires more resources circuit elements, processing units, computer memory, etc. than one that executes one batch at a time, because its stages cannot reuse the resources of a previous stage. Moreover, pipelining may increase the time it takes for an instruction to finish. An instruction pipeline is a technique used in the design of computers to increase their instruction throughput (the number of instructions that can be executed in a unit of time). The basic instruction cycle is broken up into a series called a pipeline. Rather than processing each instruction sequentially(one at a time, finishing one instruction before starting the next), each instruction is split up into a sequence of steps so different steps can be executed concurrently (at the same time) and in parallel (by different circuitry).Pipelining increases instruction throughput by performing multiple operations at the same time(concurrently), but does not reduce instruction latency (the time to complete a single instruction from start to finish) as it still must go through all steps. Indeed, it may increase latency due to additional overhead from breaking the computation into separate steps and worse, the pipeline may stall (or even need to be flushed), further increasing latency.

A. Flowchart



IV. CONCLUSION

From introductory survey it can be conclude that to transmit high speed data serial implementation is not preferred because slow throughput. So, pipeline method is used to reduce time. CRC provide flexibility and also increase accuracy in data transmission. CRC is very useful for error detection during data transmission and reception. CRC method can detect error correctly and have capability to correct and retransmit it. Thus the high speed design of CRC Encoder and Decoder Based on FPGA is one of the most efficient than any other method, pipeline method saves time for transmission which improve speed, efficiency, throughput as compare to other transmission method.

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