Logic Gates in a Single Integrated Circuit

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Abstract— The basic concept of logic gates should be clearly built up among the beginners in the field of digital electronics, since logic gates are root of every digital electronics. The newly designed system consists of all the seven logic gates. Adequate number of logic gates are implemented in this system to design the logic circuits. There are 8x (OR, NOR, AND, NAND, XOR, XNOR) and 9x(NOT) gate. This IC is designed as per standard cell design, such that VDD and GND is connected as per standard cell design whereas VDD and GND is commonly connected to avoid unwanted connections for each blocks. This IC is designed at 250nm design style. This IC had been designed with an objective to reduce the number of IC used in designing of digital circuits. Unlike FPGA is much advance in field of digital electronics but it costs huge and the designer requires the knowledge of HDL languages, which is not possible for a beginner to learn without the concept of digital electronics. Since this system is highly portable and easy to use and the connections are very simple.

Key words: FPGA, GND, HDL, HA (Half Adder), HS (Half Substractor), IC, VDD

I. INTRODUCTION

The digital circuits are the most important blocks in integrated circuits. For compact digital circuits and ICs, good designs are required [1].To accumulate the logic gates and the logic circuits standard cell design is preferred commonly. So the main option for the digital circuit is CMOS devices. In CMOS Digital circuits there are many types of logic families are available. The most used logics are static CMOS and dynamic CMOS. But these are having different constructions. The static CMOS circuits are constructed by both NMOS and PMOS devices. The logical operation evaluated by the combination of input values [2]. All the CMOS gates are implemented in rectangular chip, whose size is 250nm.The semiconductor industry has witnessed an explosive growth in sophisticated multimedia-based applications integrated with electronic gadgetry since the last decade. Since this chip is designed in such a way that the power consumption is less, and the operating voltage of the chip is 5volt DC. Since this system has been designed to reduce the cost of ICs used while designing logic circuits by the beginners. This system doesn't have logic cells and memory element so HDL coding like FPGA is not possible.

II. INDENTATIONS AND EQUATIONS

A. Truth Table

For OR Gate-

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

For AND Gate

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

For NAND Gate-

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

For NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

For NOT Gate-

A	Y
0	1
1	0

For XOR Gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

For XNOR Gate-

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Above table describes the truth table of each logic gates implemented in the chip whereas the Boolean expression of each logic gates are mentioned below

III. FIGURES & TABLES

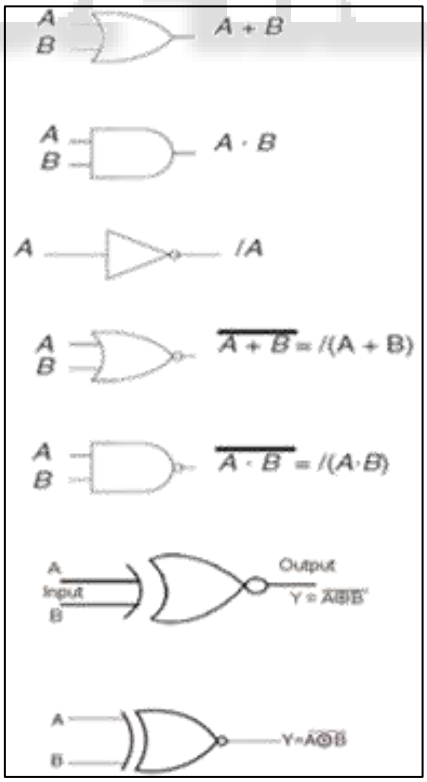

Fig. 1: Logic Gate Symbols and Boolean Expression

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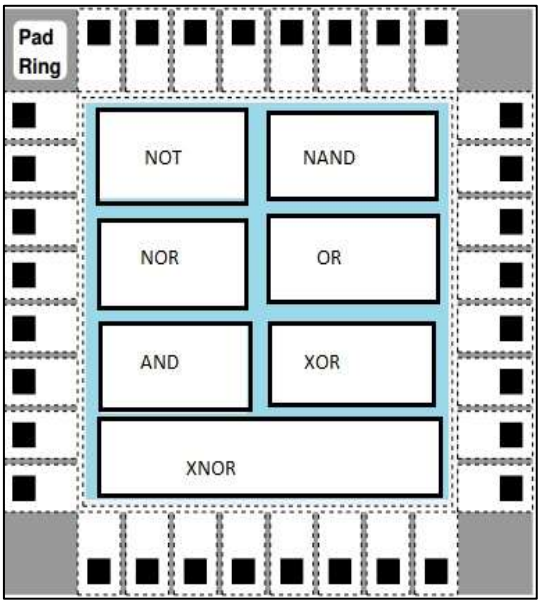

Fig. 2: Block diagram of the IC showing all it's Components

Fig-2 shows the block diagram of the IC that layout is designed as per the block diagram.Since different blocks are indicated in figure 2 via which the layout is created.

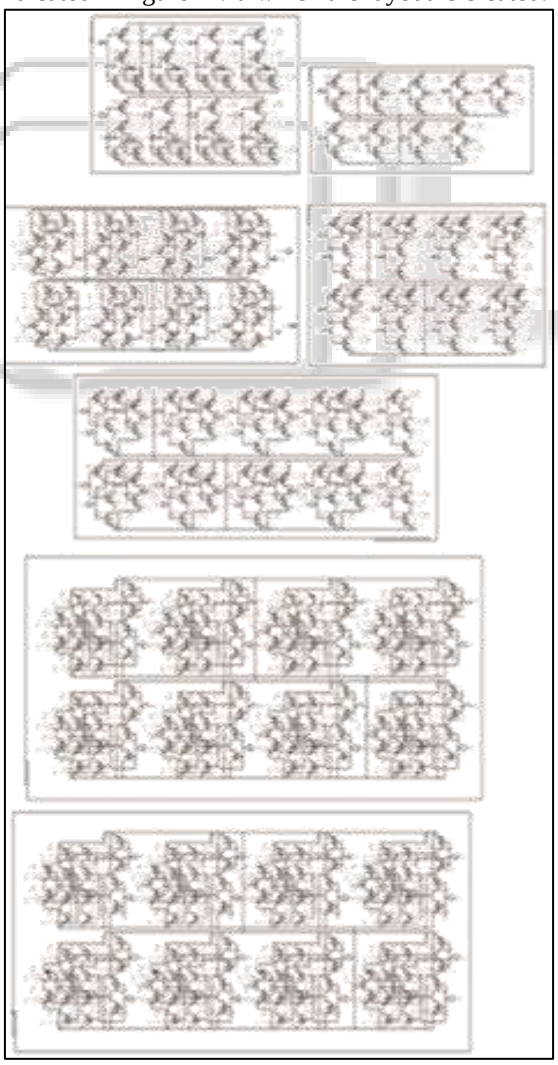

Fig. 3: Schematic Block of Logic Gates

Fig-3 describes schematic diagram of the IC clearly all the 7 logic blocks are mentioned in the schematic diagram and the software used for designing the schematic is Tanner S-Edit v16.0.

Well	
Minimum well size	12λ
Between wells	6λ
Between N-well and P-well	0λ
Minimum well area	$144\lambda^2$
Polysilicon1	
Polysilicon1 width	2λ
Between polysilicon1s	3λ
Between polysilicon1 and metal	N/A
Minimum polysilicon1 area	$4\lambda^2$
Metal1,2,3,	
Metal width	3λ
Between metals	3λ
Between metal and other metal	N/A
Minimum metal area	$9\lambda^2$
Via1,2,3	
Via width	2λ
Minimum via area	$4\lambda^2$

Table 1: List of Fundamental Rule of Designing an IC Layout

Since the chip works on 5 volt and power dissipation is 2.5 watt by using formula P=V*I, where V=5volt and I=500ma.This chip contains total 164 pins 41 on each side where 8x(OR,NOR,AND,NAND,XOR,XNOR), 9x(NOT) gate, VCC and GND are implemented.

The XOR-XNOR circuits are basic building blocks in various circuits especially- Arithmetic circuits, Multipliers, Compressors, Comparators, Parity Checkers, Code converters, Error-detecting or Error-correcting codes and Phase detectors[3].

IV. Discussion

A. Power

Power is a vital resource. Hence the designers try to economize on it when designing a system. In CMOS circuits most of the energy consumed is due to switching activity. The number of nodes in the circuit, the stored energy per node and the number of switching operations per second, all contribute to the total power consumption. Power dissipation is dependent on the node capacitances (made up of gate, diffusion, and wire capacitances), switching activity and circuit size. In a CMOS circuit the majority of the energy dissipation is expressed by:

$$\text{Energy}=\sum \tfrac{1}{2}cv^2$$

There are four causes of power dissipation: dynamic switching power due to the charging and discharging of circuit capacitance, leakage current power from reverse biased diodes and sub-threshold conduction, short-circuit current power due to finite signal rise/fall times. There are following three major components of power dissipation in complementary metal oxide semi- conductor (CMOS) circuits[4].

1) Switching Power

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Power consumed by the circuit node capacitance during transistor switching.

2) Short Circuit Power
Power consumed due to the current flowing from power supply to ground during transistor switching.

3) Static Power
Power due to leakage and static currents.

B. Energy

Energy per cycle of a circuit is a key parameter for energy efficiency in VLSI applications. Because computing workload is characterized in terms of clock cycles, this measure directly relates energy consumption to the workload. Before considering the energy consumed by a circuit, we start by examining the total energy per cycle (Etot) of a single gate, which is composed of dynamic energy[4].

V. RESULT

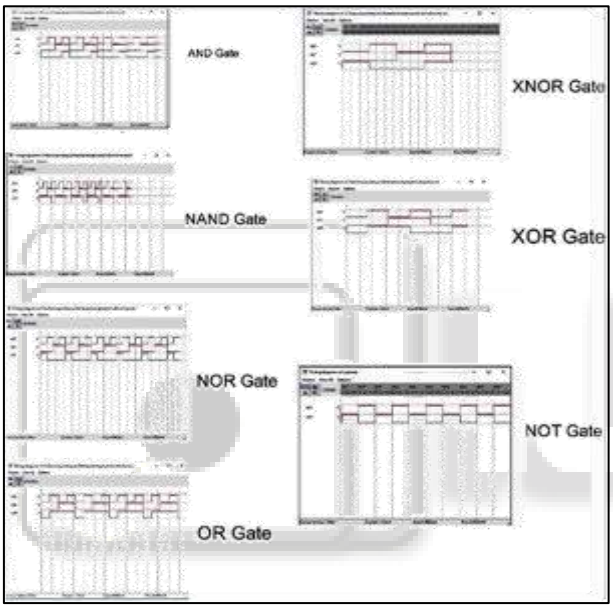

Fig. 4: Simulation of Logic Gates

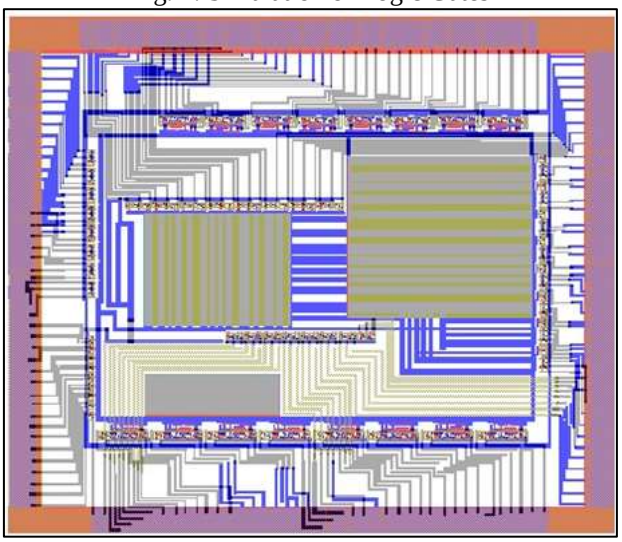

Fig. 5: Transistor Level Layout of the IC

Above figures Fig.4 and Fig.5 points out the simulation of single logic gate and final transistor layout of the IC. In Fig.5 all the layers are indicated which are used for designing the layout of the IC.

A. Setting and Installation

Before start drawing the schematic circuit, all the setting of the Electric VLSI Design System must be done properly. These include the installation of external simulator of T-Spice, setting of spice engine and its path, technology and scale used, S-Edit and Wave form viewer DSCH v2.0.

B. Verification Process

As mentioned earlier, physical verification process is an essential procedure. The schematic diagram and layout design can be checked through DRC. It is recommended that the schematic diagram is free of warning and error before designing its layout. This process will check the number of exports, ports, transistor size between schematic and the layout. Error may occur if they are not consistent. While running the LVS, the library names for both schematic and layout have to be same and place under the same group. This is to ensure that the software compares the correct library[5].

VI. CONCLUSION

This chip will play and important role in field of logic design, because it has all the basic logic gates in a single IC. So it will be an advantage for the beginner, they do not have to get meshed up with lots of IC to design their projects. This system is highly portable. Since this is the cluster of logic gates it cannot overcome the FPGA toward its speed and processing capacity. This IC need to be placed on a special PCB in which all of its connections are made through i/o ports. This chip will able to design all logic circuits as per logic design standards.

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