Low Power 9T SRAM Cell by using Power Gated Technique

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Abstract— RAPBG techniques are obtainable in this paper to minimize the power consumption. Scheming memories with dynamic voltage scaling (DVS) capability is important since important active as well as leakage powers can be reduced by voltage scaling. Ultra-dynamic voltage scaling is to scale the supply voltage by using assists circuits for diverse modes of the cell operation. Write assist circuits are intended to improve the write margin of the SRAM cell. In this paper three write assist circuits and two read supports circuits have been designed. First one is Capacitive W-AC approach to reduce the level of cell supply voltage accordingly when word line is allowed so as to make power reduction. Second scheme is Transient Negative Bit-line Voltage write assist scheme executes write operation without using any on-chip or off-chip voltage sources. Read assist circuits are calculated for basic cell of SRAM to read the data from the cell without changing the cell data with low power consumption and high data transferal speed. Reconfigurable assist circuits provide the necessary flexibility for circuits to adjust themselves to the requirements of the voltage range that they are operating in. In this paper finally implemented 9T SRAM cell with efficient data transfer with high speed with less power consumption in 45nm with RAPBG Technique in which supply voltage could be changed for different modes of action of SRAM Cell.

Key words: UDVS, Tran-NBL, Capacitive W-AC

I. Introduction

Static Random Access Memory (SRAM) comes below classification of volatile memory. In recent year's high speed and low-power circuit design fast more importance in research area. Since tremendous development in VLSI skills, the designing of high speed and low power devices such as portable electronic gadgets is most operational field in industry.

So energy saving is a key point in manipulative the electronic circuits. So Robust SRAM with PMOS Access and built in feedback (RAPBG) technique is a method to reduce energy consumption by regulating the system supply voltage over a wide range dependent on the performance of operation must. LVVT is required for systems with time-varying limits like output voltage or frequency. In modern ICs, caches are occupying more area in scheming on-chip memories. So, on chip memories accordingly cause more energy consumption. For the RAPBG techniques stated above, it is required to have the on chip memories are capable of working on a wide voltage range. An SRAM planned for operation in sub-threshold accessible in this paper.

This paper first deliberates voltage scaling and design issues, operation of basic SRAM cell and write assists patterns.

II. Proposed & Operation of SRAM Cell

This brief suggests a novel power-gated 9T (PG9T) static random access memory (SRAM) cell that uses a read-decoupled access buffer and power-gating transistors to perform reliable read and write operations. The proposed 9T SRAM cell uses bit including to achieve soft error immunity and uses a column-based virtual VSS signal.

Modes of the cell are

- Write mode.(supply should less or bit-line should negative)
- Read mode.(cell supply voltage should high)
- Standby mode.(stability should high)

A. Write Mode

Writing the data in to the cell pointers to latching in the cell. This latching occurs created on threshold levels of both inverters linked in back to back so as to store the data. For easy write actions there are so many write assist arrangements to have low power consumption.

1) Write Driver Circuit

In order to read the write driver circuit efforts the suitable data values onto the bit line true and approval lines. Since the primary objective data from an SRAM, the Data must write into memory first. The four vertical devices in series are frequently referred to as a gated inverter. When write enable is declared high is to drive a "0", the NFETs and PFETs may be also sized, rather than the typical two to one ratio. Write circuitry and its waveforms are shown in "Fig1"and "Fig2" respectively.

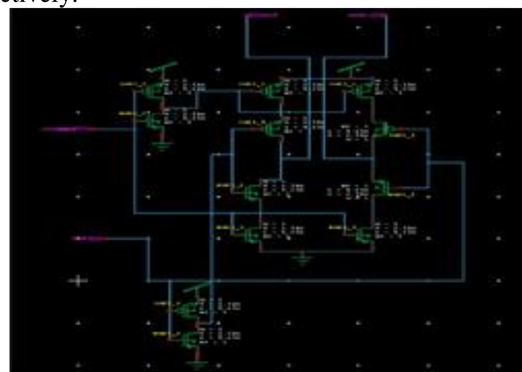

Fig. 1: Write driver circuit

Fig. 2: Waveform of Write driver circuit

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2) Write assist schemes

Control of process limit becomes extremely difficult by Scaling supply voltage and sizing of transistors. So each time scaling the supply voltage manually is not value to achieve low power constraint but write circuit writes the data into SRAM cell when power of the cell stored data is less than that of write data. For that cell supply voltage should less than that of write circuitry supply voltage. Write assist paths can solve this problem. In this paper three write contribution arrangements have been used to make write data to be written in to the cell.

- Capacitive W-AC (capacitive write assist scheme)
- Transient-NBL (transient-negative bit line scheme)
- NBL scheme on the source of the write circuit

a) Capacitive W-AC(Capacitive Write Assist Scheme)

In this pattern data can be written with high WM by altering the strength of the cell. Cell supply is climbed by using column write assist circuit so as to reduce the cell strength. Lowering the SRAM cell voltage supply reduces the current to the pull-up PMOS device. As result, this supports the SRAM"s write operation. In this method the bit-cell supply is lowered below the word line level by capacitive charge distribution scheme.

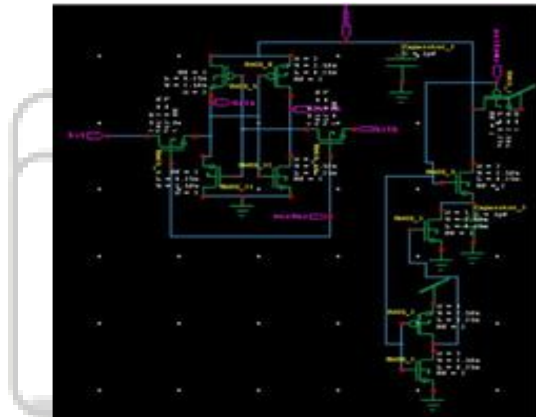

Fig. 3: Capacitive LVVT circuit

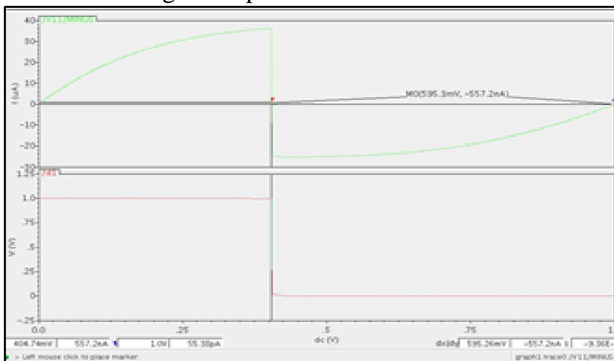

Fig. 4: Waveforms of Capacitive W-AC circuit

Here by DC analysis is done to get N-Curves shown in "Fig 4" when word line is high. Capacitive WA outline is used to scale supply to reduce cell stability.

b) Transient-NBL (transient-negative bit line scheme) write circuitry

This is the second write assist outline to make very easy write operation. Main aim of order is undershooting bit line to deliver negative source voltage to access transistor so as to run high channel width to write the data early means WM can be improved.

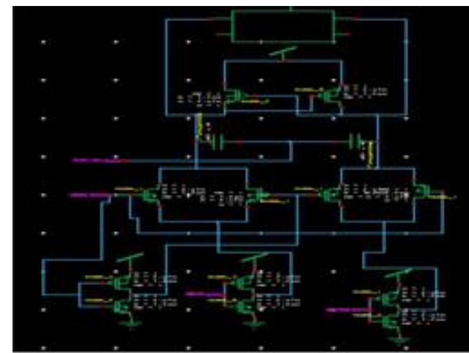

Fig. 5: Transient-NBL write circuit

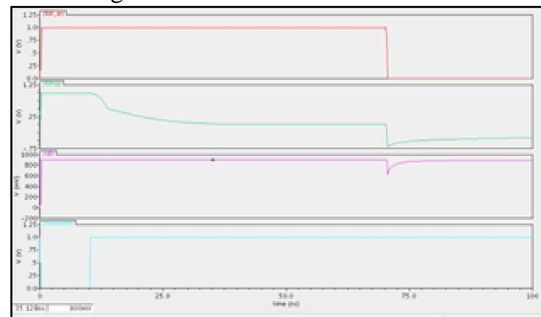

Fig. 6: For Cell supply voltage is 900mV

From "Fig 6" data can be driven into the cell is 1 when NBL driver circuitry make bit line is negative. In this transient negative bit line pattern write operation is achieved by increasing the power of SRAM pass transistor. When supply voltage of the cell is 900mV so that strength of the stored data is more than write data. So for 0 is written when Bit-en low and cell is not able to key. So cell strength has been compact to latch the state of the cell.

c) NBL scheme on the source of the write circuit

In this scheme write of data is accomplished by negative the bit line as before but change of this scheme is applied the negative bit-line power on source of the driver circuitry in its place of using coupling operation inside the driver circuitry.

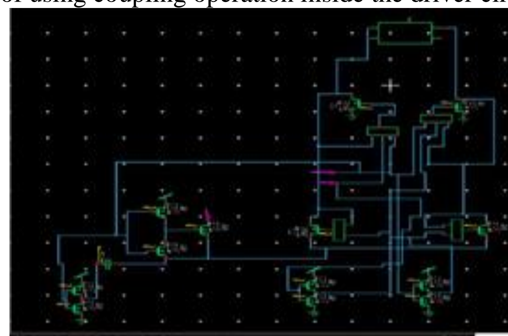

Fig. 7: Source coupled NBL write circuit

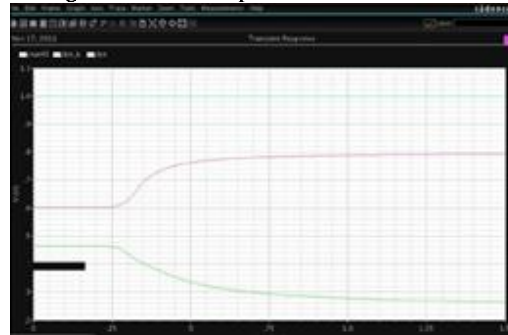

Fig. 8: Waveform of source coupled NBL write circuit

From above "Fig 8" data can be focused into cell is 1using NBL driver circuitry.

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B. Read Assist Schemes

To improve both stability and performance of SRAM cell, it is main that the Bit line capacitive loading should be as low as possible. In this section we examine a new read-assist scheme for cell that will nullify the drawbacks of local sense amplifier. The proposed schemes improves the concert of sensing circuitry by amplifying the BL voltage drop and while sinking the BL voltage swing which results in significant power fall. Reduction in cell VDD with respect to the original scheme causes reduction in leakage power dissipation. These hitches can be overcome by following Read assists schemes.

1) Proposed Read Assist scheme for 9-T SRAM Cell

Here while performing write operation to cell write driver circuitry is needed lengthwise with to perform read operation following read kit is needed

- Sense amplifiers
- Isolation circuitry
- Pre-charge circuitry
- SRAM Cell

Operation: while execution read operation first isolation circuitry going to isolate sense amplifier then pre-charge circuitry pre-charge the bit-line so as to produce possible error to sense data using sense amplifier.

Fig. 9: Read assists Scheme with 6-T

2) 9-T cell with all peripheral circuitry to write and read totally

Here RAPBG System is used to make read and write operation on cell with less power consumption. Proposed Technique is used by which cell solidity can be adjusted affording to the cell operation so that power degeneracy can be very low.

Here N, P Sense amplifiers are used to improve speed of operation by reducing sensing delay. So Speed and power intake requirement for any system can be attained using this read assist scheme.

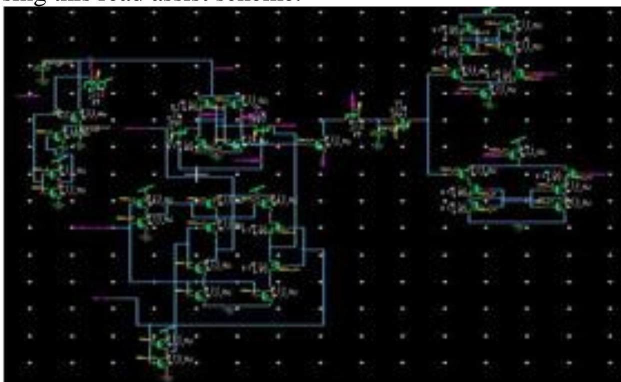

Fig. 10: Read assist Scheme with 9-T

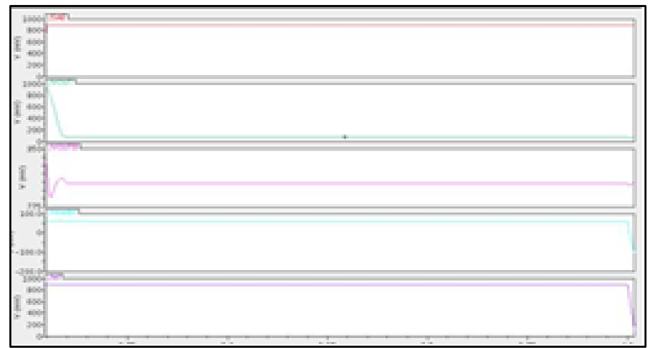

Fig. 11: Waveforms of Read Assist Scheme

Here Data which is stored in SRAM cell can be sensed using P, N Sense amplifiers after pre-charge operation is performed which is shown in "Fig 11".

C. Standby Mode

Here write enable line should be zero. So two transistors in 9T SRAM cell are in off condition. Current is generally smooth between supplies to ground. We designed circuit to reduce leakage current and is designed in 45nm technology with sub-threshold voltage of 0.7V. Until and unless threshold voltage is 0.7V transistor is not switched ON.

III. LAYOUTS

Fig. 12: Layout of 9T SRAM cell

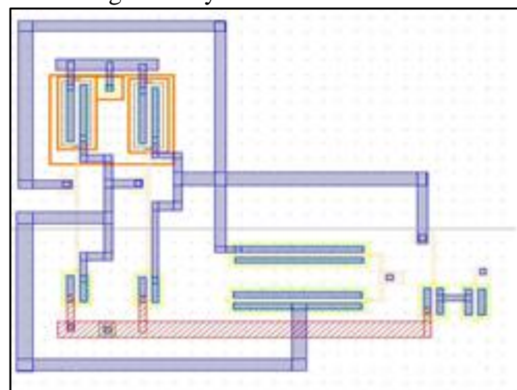

Fig. 13: Layout of 9T SRAM cell

IV. RESULTS & DISCUSSION

A. Power Calculations for 9-T SRAM Cell

The delay and power controls are done on this schematic 9-T SRAM cell

1) Calculation of delay

Write to bit b =52.33ps

Write to bit = 26.33ps

- Calculation of power

Condition	Power in watts
Initial	37.84×10^{-15}

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Write -"1"logic	123.5×10^{-15}
Read-"1" logic	32.3×10^{-15}
Write-"0" logic	118.4×10^{-15}
Read-"0"logic	32.8×10^{-15}

Table 1: Calculation of power

From above "Table 1" it is clear that power consumed by SRAM cell in write operation is more when likened to read operation.

2) Delay and leakage currents for 9-T SRAM cell are calculated. Cell is sized according to better write and read margins.

a) Delay calculations

- Write in to bit-line=42.02ps.
- Write into bit-line-bar=35.4ps.

b) Calculation of currents

I read=60.2uA, I leakage=57.4pA.

Here leakage power of the cell= $I_{leakage}$ x supply voltage (in standby mode) =3.21 x 1 =3.21 uW.

- Calculation of power

Conditions		Power (watts×10^{-15}
Write	Logic-1	102.2
Write	Logic-0	92.3
Read	Logic-1	52.3
Read	Logic-0	42.9

Table 2: Calculation of power

From above "Table2" we can achieve that power consumed by SRAM cell for write operation is more than read operation. The write assist schemes to reduce the power consumption because we are planning low power SRAM so power consumption should less.

- Calculation of power dissipation

Name of the Write Assist Scheme	Write Margin (WM)	
	Write Trip Voltage	Write Trip Current
92.3	Write	Logic-0
Capacitive W-AC	0.69V	5.8uA
Transient-NBL	0.62V	3.1uA

Table 3: Calculation of power dissipation

c) Write margin calculations

Write margin describes how fast the data is going to write and read margin is clear to know how fast the data is interpretation from the cell.

- Write Margin

Supply voltage of the cell	Power dissipation(pW)
1 V	50.4
0.5 V	52.9

Table 4: Write margin

These values are calculated by using N-curves of the cell drawn by varying one node voltage from 0 to supply voltage and by doing DC analysis.

V. Conclusion

A co-designed SRAM cell topology, layout and assist schemes to effectively enable a Wide Voltage Range (WVR), 0.35V to 1.2V, operation of a 32Kb SRAM across all process corners. It demonstrate that D3SBM write assist scheme proposed in this work can be easily combined with conventional schemes to extend operation range of WVR SRAMs. The proposed Figures of Merit to benchmark different implementations of Low Voltage and Wide Voltage Range SRAMs. It shows that the schemes and methods proposed in this work provide more levers of design optimization to SRAM designers and enable significantly better WVR SRAM design. The proposed FoMs can help designers to make optimal design choices and improve energy efficiency. The techniques proposed in this work can be combined with other methods to enable up to 6X better FoM performance than the reference.

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