Designing of a CMOS NAND Gate using INDEP with Bi-Triggering (Trig01) Method

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Abstract— In deep submicron process power consumption is one of the major concerns in CMOS circuits. Moving to finer technologies for high transistor density and smaller equipment size as per the market demand, leakage power is increasing rapidly, due to reduced voltage and oxide thickness. In this paper a new leakage power reduction technique is proposed which is a combination of two approaches namely INDEP Approach and Trig01 (Bi-Triggering) Approach. The simulation is done at 130nm process technology using Mentor Graphics Back End Tool with Pyxis Schematic 10.5 version on Linux Operating System. Significant power reduction is achieved with reduction in propagation delay and power delay product.
Key words: EH-WSN, MS, ECR, ERR, ICGS, ICA, GS

I. INTRODUCTION

The modern technologies move towards smaller, faster, and cheaper computing systems. This can be done by increasing the density of the device and operating frequency through VLSI technology scaling. Moving to smaller feature size in DSM process, leakage power consumption came up with major importance in designing CMOS VLSI circuit. During the idle state the smaller size transistor leaks more power through the source, directly affecting the battery life of the device. Power dissipation comprises two components: static and dynamic components. Energy per operation continues to improve with process and supply scaling because dynamic power is approximately proportional to the square of supply voltage as well as proportional to capacitances of device. Despite the use of low power supply voltage, total power consumption is increasing every technology generation because dynamic power consumption increases due to higher operating frequencies and higher transistor density while leakage power consumption increases exponentially due to reduced gate length, threshold voltage, oxide thickness, and higher transistor density. The static power is increasing as the feature size decreases, which is dominating the consumption of total power in lower feature size CMOS circuits.

In this paper, firstly the techniques previously described for leakage power consumption of NAND Gate logic are designed using 130nm process technologies. Then, a new NAND gate design is proposed by combining the two design approaches.

The structure of the paper is organized as follows: in section II the work related to leakage power reduction techniques is discussed. In section III, the design approach proposed for the NAND gate is described. In section IV, simulation results and discussion are evaluated. Finally, the conclusion in given section V.

II. LITERATURE REVIEW

In this section, a brief review of previously proposed leakage power reduction approaches is given.

A. Sleep Approach

It is one of the most common leakage power reduction technique in Deep Sub Micron technology.

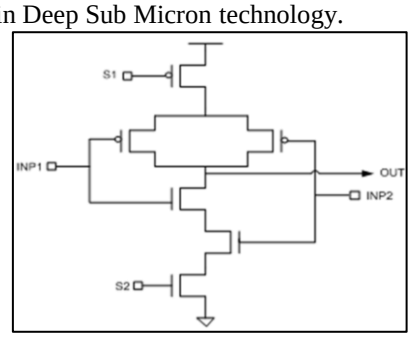

Fig. 1: NAND gate with sleep transistor technique

In this approach sleep transistors (a pMOS and an nMOS) are added in between the power supply and pull-up network and between pull-down network and ground for mitigating the standby leakage currents as shown in Fig. 1. During active mode sleep transistors are turned on and are turned off during standby mode. The leakage power due to leakage currents in standby mode is reduced in technique by adding sleep transistors which cuts off the logic networks from the power supply and ground. The output logic is not achieved properly in this approach.

B. Lector Approach

In Lector approach two more transistors known as LEakage Control transistor (pMOS and nMOS) are added in between the pull-up and pull-down network as shown in Fig. 2. The idea behind these two leakage control transistors (LCT) is that for any input combination one of these two transistor always remain near the cut-off voltage. Since one of the LCTs is always near its cut-off region, increment in path resistance from Vdd to GND is causes by leakage control transistors, which reduces the leakage current. Output logic is not achieved properly in this technique.

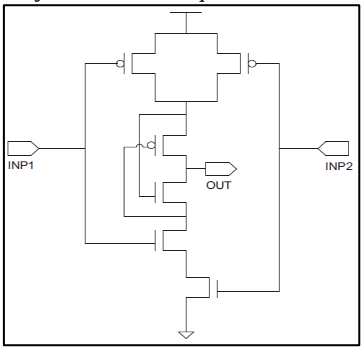

Fig. 2: Lector NAND Gate

C. INDEP Approach

In INDEP approach two more transistors called INDEP transistors (an nMOS and a pMOS) are added in between pull-up and pull-down networks of the CMOS logic circuit as shown in Fig. 3. The output node is formed by connecting the drain nodes together of the INDEP transistors MP1 and MN1. The source terminals of the transistors are attached to drain terminals in the pull up network and the pull down network. V_0 and V_1 are the input signals given to the MP1 and MN1 transistors. INDEP transistors threshold voltage is kept similar to the transistors of pull up/pull down network. This creates single threshold operation throughout the circuit which removes the difficulty of operating circuit with multiple threshold voltages.

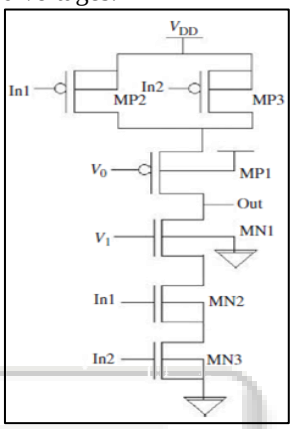

Fig. 3: INDEP CMOS NAND Gate

D. Trig01 (Bi Triggering) Approach

In Bi Triggering (Trig01) approach two more transistors (a pMOS and nMOS) are added to the circuit and are used as a Bi-Trig Control circuit. Thus the entire circuit is driven with the method voltage dividing. The Bi mode helps in reducing the ideal current and to drive the large capacitive load full mode operation is used. The control circuit is added in between the power supply and the pull up network. Here with the use of pMOS and nMOS transistors the operating voltage is divided into two parts. These transistors are given separate inputs. The input and output are directly applied to the CMOS circuit and obtained from the circuit. Bi-Trig control circuit control the half mode power output by making either pMOS or nMOS ON or OFF using the trig pulse 0 and 1 or 1 and 0.

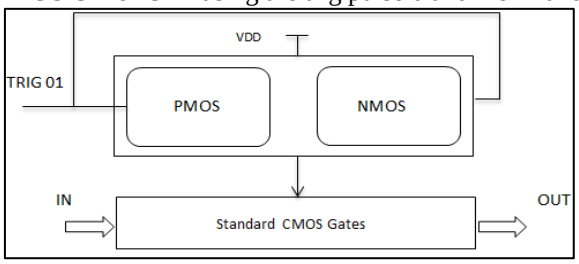

Fig. 4: Trig01 Approach Block Diagram

III. PROPOSED WORK

In this section, a novel low-power high performance modified NAND gate circuit approach is presented. For better leakage reduction a circuit is proposed which is a combination of two approaches: INDEP Approach and Trig01 Approach. Using the idea behind the INDEP approach two transistors called the INDEP transistors are added in between pull-up network and output terminal and in between output terminal and pull-down network of the circuit. The output is obtained by connecting the drain terminals of these added transistors. V_0 and V_1 are the input signals given to the INDEP transistors. The Boolean logic at input terminals V_0 and V_1 controls the operations of these INDEP transistors.

Using the concept of Trig01 approach, nMOS and pMOS transistors are added in between the pull up network and the power supply. These transistors used as Bi-Trig control circuit. This divides the given operating voltage to the circuit into two parts as in voltage divider method. These extra added transistors are given separate inputs. The input and output are directly applied to the CMOS circuit and directly taken from the circuit.

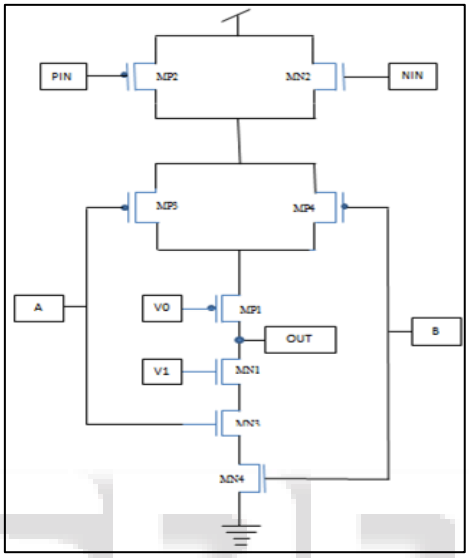

Fig. 5: Proposed NAND gate circuit: INDEP with Trig01 Approach

Relying on the output logic state V0 and V1 are connected to In1 and In2. When In1=In2, then V0 and V1 are connected to any input signal. In 01 and 10 state, V0 and V1 are connected to input signal such that the MP1 and MN1 transistors are both ON and complete logic is obtained at the output.

pMOS and nMOS are given trigger pulse (clock pulse). For half mode power output either pMOS or nMOS is ON. For a full mode operation the pMOS and nMOS both are ON i.e. they are in closed loop. The extra added INDEP transistors creates effective transistor stacks in the path from power supply to ground which increases the resistance of the path from Vdd to GND which in turn reduces the CMOS logic circuits leakage current. Combining both the approaches there is a significant decrease in the leakage power consumption, propagation delay and power delay product.

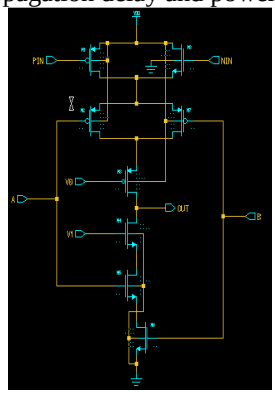

Fig. 6: Mentor Graphics file Proposed NAND Gate Design

Similarly using the proposed approach other gates such as AND, OR, NOR, XOR, etc. and Flip Flops like D, T, RS, and JK Flip Flop can be observed.

The NAND Gate circuit designed in Mentor Graphics and its waveform are shown below.

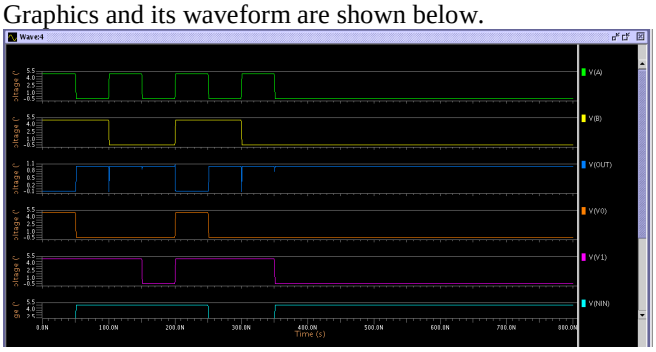

Fig. 7: Waveform of Proposed NAND Gate Design

IV. Simulation Results

In this section, the comparison of the proposed approach with some previously existing technique such as sleep, LECTOR, sleepy LECTOR, INDEP, and Trig01 Approach in terms of Leakage Power Dissipation, Delay, and PDP. The comparison is shown in Table I, and it concludes that the proposed NAND gate has the least leakage power dissipation. Propagation delay and power delay product are also reduced. The proposed NAND Gate is most efficient in terms of power behavior.

The simulation is performed in Mentor Graphics Back End Tool with Pyxis Schematic 10.5 version on Linux Operating System with 1V power supply at 130nm technology at temperature 27^0C. Figure 8, 9, 10 shows the comparison graph of different NAND Gate design Approaches.

Approaches for NAND Gate	Leakage Power Dissipation (pW)	Delay (pS)	PDP(J)
Base NAND	8.132	172.013	$1398.8*10^{-18}$
LECTOR	5.512	346.847	$1911.8*10^{-18}$
Sleepy LECTOR	4.924	408.412	$2011.0*10^{-18}$
INDEP	5.491	145.186	$797.2*10^{-18}$
Trig01	6.002	173.316	$1010.2*10^{-18}$
Proposed (INDEP+Trig01)	3.835	150.075	$575.5*10^{-18}$

Table 1: Comparison of Power, Delay, and PDP of Different NAND gate Design Approaches with Proposed Approach

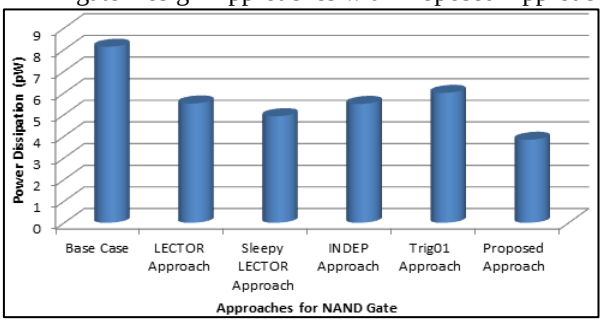

Fig. 8: Comparison of Power Dissipation of Different approaches with proposed approach

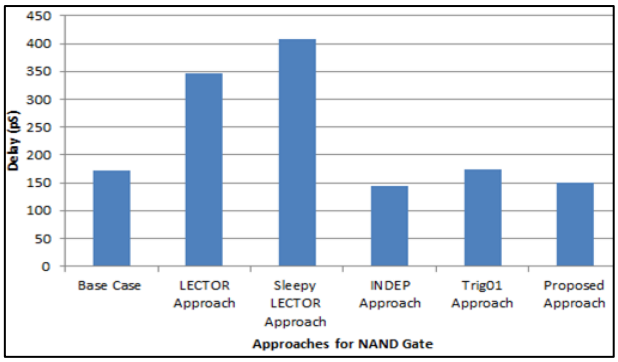

Fig. 9: Comparison of Delay of Different approaches with proposed approach

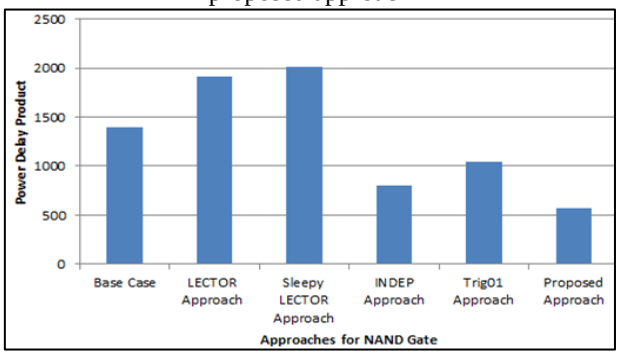

Fig. 10: Comparison of PDP of Different approaches with proposed approach

V. Conclusion

In this paper, we have proposed an efficient NAND Gate design approach for leakage power reduction which is a combination of INDEP approach and Trig01 approach. The simulation result demonstrates that proposed approach is efficient in decreasing leakage power dissipation, delay, and power delay product. The proposed NAND gate can be used for designing Flip Flops, Multiplexers, Adders, etc for reducing the leakage power dissipation and increasing the performance. The leakage power dissipation in NAND gate can be further mitigated by modifying the conventional NAND gates by adding or removing transistors.

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