Analysis of High Performance & Low Power Shift Registers using Pulsed Latch Technique

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Abstract— In this work, the performance of shift registers is improved using pulsed latch technique. In high speed and low power VLSI applications where heavy pipelining is required, low power edge triggered flip flops are used. The replacement o flip flop with pulsed latch has shown great success in low power VLSI applications. The proposed circuit has been designed using Tanner Tools v 14.1 in CMOS technology. The pulse latch technique reduces the power consumption significantly in the designed circuit and there is also an improvement in power delay product. The proposed circuit also require less number of transistors for its implementation as compared to conventional version.

Key words: Shift Registers, Low Power, Pulsed Latch, D Flip Flop

I. INTRODUCTION

In SOC's (System On Chip), many techniques have been used to diminish the dynamic power of overall circuit which impose physical constraints or depend heavily on logic function of circuit. Dynamic power is mainly consumed by clock network. So techniques to reduce the power in clock network actually minimize the dynamic power significantly. Techniques such as adding smaller clock buffers or reducing the wiring capacitance of overall circuit or by clock gating can be used. The dynamic power of clock network can be large even with this technique since commonly used state element in the design is flip flop used as a register [1]. For mobile devices, where power consumption is the prime concern with high speed of operation, there is requirement of low power flip flops in designs. Shift registers find extensive applications in areas such as digital filters, communication receivers and image processing IC's [2], [3], [4].

A flip flop is sequential edge triggered circuit which is integral part in most applications [5]. In particular, sequential edge triggered circuits consists of combinational block in between D flip flop which is commonly used in ASIC applications. Mostly flip flop is composed of back to back latches with clock and inverted clock input to respective latches. However the main drawback of using flip flop is large power dissipation, counting upto 50 percent of overall power of circuit. Hence, there is requirement of replacing the flip flop with more efficient circuit which has same functionality while achieving low power, area and robustness to PVT variations [6]. Pulsed latch technique is one of the most practicable solutions to this problem. Rest of the paper is organized as follows: Section II presents the principle of pulsed latch technique. In section III, shift registers have been implemented using pulsed latch technique. Simulation results are given in section IV and Conclusions are summarized in section V.

II. PULSED LATCH METHOD

Flip-flops impose major overhead in terms of delay, clock load, and area as compared to the latches. However this is certain since flip-flops are mainly constructed by connecting two level sensitive latches in a master-slave fashion as shown in Fig. 1.Hence, there is requirement of replacing the flip flop with circuit design which has same functionality. Pulsed latch technique is one of the most feasible solutions to this problem.

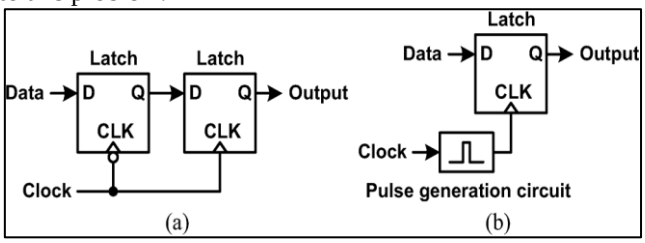

Fig. 1: (a) Master-slave flip-flop. (b) Pulsed latch.

Pulsed latch technique broadly comprises of a pulse generator and a latch [7]. The most attractive feature of using pulse latch technique is that the performance of existing designs can be improved without changing the existing design style. There can be wide range of applications for pulsed latches especially in low power design where flip flop could be replaced that is in pipelining or as sequencing element or as register.

III. SHIFT REGISTER DESIGN

A master-slave flip-flop using two latches in Fig. 1(a) can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in Fig. 1(b)[6]. All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption. The pulsed latch cannot be used in shift registers due to the timing problem. The shift register consists of several latches and a pulsed clock signal (CLK_pulse).The output signal of the first latch (Q1) changes correctly because the input signal of the first latch (IN) is constant during the clock pulse width. But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.

One solution for the timing problem is to add delay circuits between latches, as shown in Fig.2(a). The output signal of the latch is delayed and reaches the next latch after the clock pulse. As shown in Fig.2 (b) the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width , but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input

signals during the clock pulse and no timing problem occurs between the latches. However, the delay circuits cause large area and power overheads.

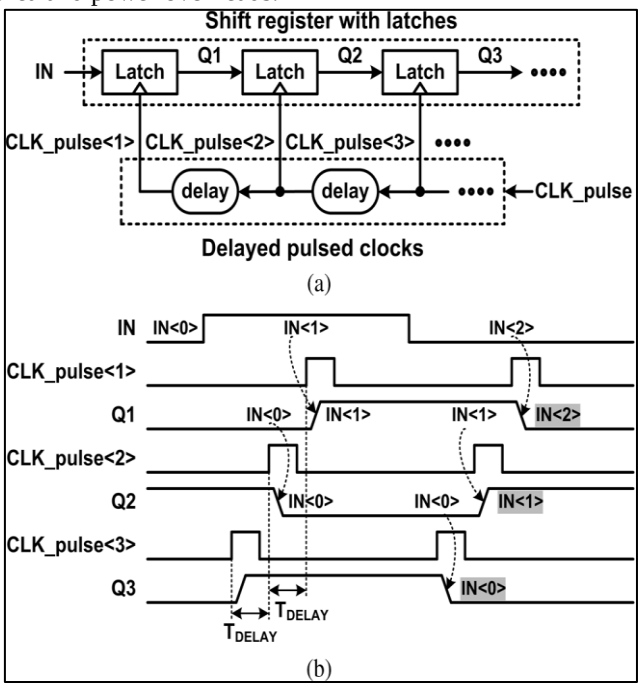

Fig.2 Shift register with latches and delayed pulsed clock signals. (a) Schematic (b) Waveforms.

Using the delayed pulse generator SISO, SIPO, PISO and PIPO is implemented. Serial in serial out shift register is capable of moving data input left or right with clock pulse and output taken from rightmost sequential element or leftmost sequential element respectively and so on.

Table 1 gives comparison of performance parameters of D flip flop and pulsed latch. It is observed pulsed latch technique reduces the power dissipation and power delay product.

	D flip flop	Pulsed latch
Power (uW)	263	142
Delay (ps)	53.11	51.8
Power delay product (fWs)	13.97	7.3

Table 1: Comparison of performance parameters of D flip Flop and pulsed latch

IV. Schematic and Simulation Results

In computer systems it is often necessary to transfer *n*-bit data items. This may be done by transmitting all bits at once using *n* separate wires, in which case we say that the transfers performed in *parallel*. But it is also possible to transfer all bits using a single wire, by performing the transfer one bit at a time, in *n* consecutive clock cycles. We refer to this scheme as *serial* transfer.

Based on this concept, we have four types of Shift registers:

1) SISO shift register
2) SIPO shift register
3) PISO shift register
4) PIPO shift register

These circuits are implemented here using pulsed latch concept.

A. SISO (Serial In Serial Out) using pulsed latch

The implementation of 4-bit SISO using pulsed latch is shown in fig 3. To avoid the timing problem, delayed pulse clock generator method is used.

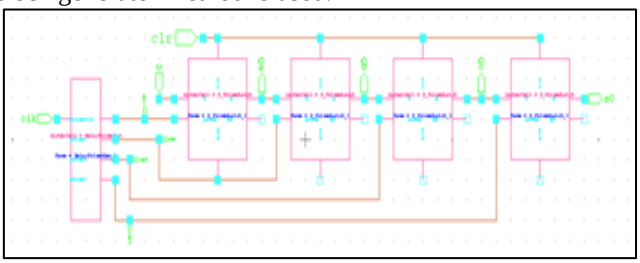

Fig. 3: Schematic of SISO using pulse latch

1) Waveform

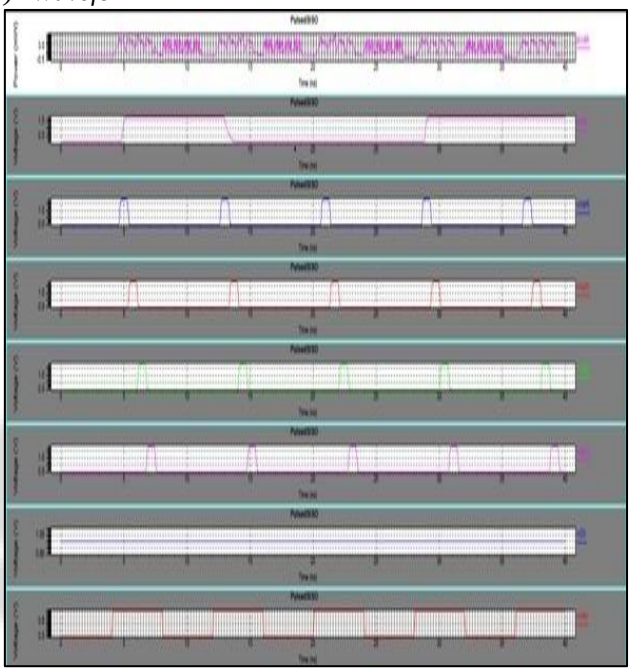

Fig. 4: Waveform of SISO using pulse latch

	SISO using pulsed latch	SISO using D flip flop
Power (uW)	259.16	514.47
Delay (ps)	29.09	53.33
Power delay product (fWs)	7.53	27.43

Table 2: Comparison of performance parameters of SISO

B. SIPO (Serial In Parallel Out) using pulsed latch

SIPO using pulsed latch employing delayed pulse clock generator technique.The input is given to first latch in same manner as SISO but parallel outputs (Q0, Q1, Q2, Q3) are taken from each latch as soon as the data is stored in respective latch.

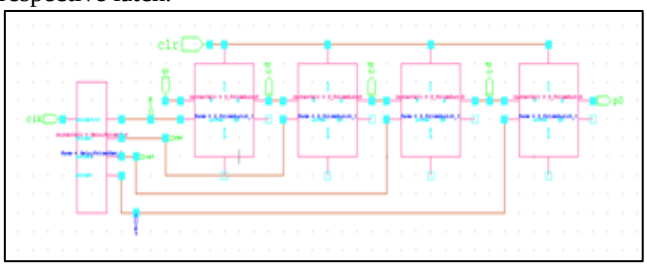

Fig. 5: Schematic of SIPO using pulse latch

1) Waveform

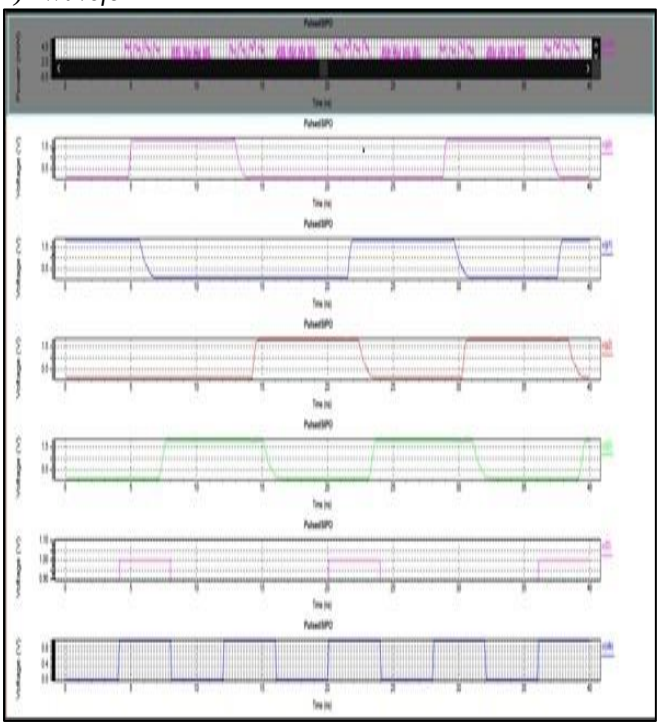

Fig. 6: Waveform of SIPO using pulse latch

	SIPO using pulsed latch	SIPO using D flip flop
Power (uW)	260.39	514.51
Delay (ps)	37.91	49.76
Power delay product (fWs)	9.87	25.6

Table 3: Comparison of performance parameters of SIPO

C. PISO (Parallel in Serial out) using pulsed latch

The implementation of PISO using pulsed latch is shown. In this D0, D1, D2, D3 are parallel input provided to each latch respectively. When control signal Shift/loadb is low or 0, input is loaded in each latch. While control signal Shift/loadb is high or 1, the shift operation is done. The output is taken out serially from last latch.

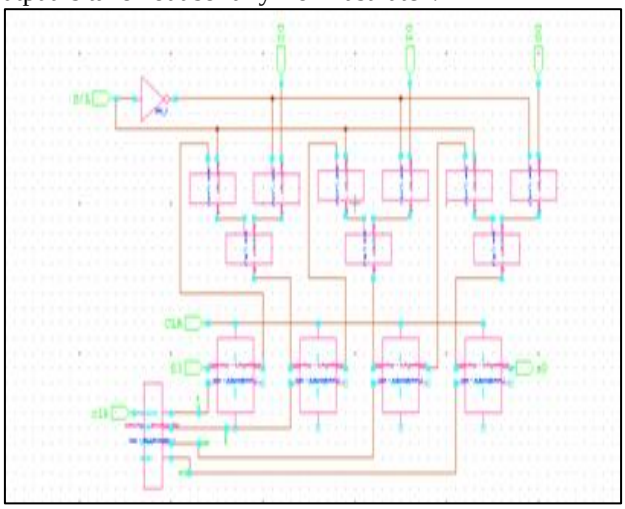

Fig. 7: Schematic of PISO using pulse latch

The control signal *Shift*/*Load* is used to select the mode of operation. If *Shift*/*Load* = 0, then the circuit operates as a shift register. If *Shift*/*Load* = 1, then the parallel input data are loaded into the register.

The input to this register is given in parallel i.e. data is given separately to each flip flop and the output is collected in serial at the output of the end flip flop. The input data is connected individually to each flip flop. Here D0, D1, D2 and D3 are the individual parallel inputs to the shift register. In this register the output is collected in serial. The output of the previous flip flop and parallel data input are connected to the input of the next flip flop. A Parallel in Serial out (PISO) shift register converts parallel data to serial data. Hence they are used in communication lines where a number of data lines are multiplexed into single serial data line.

1) Waveform

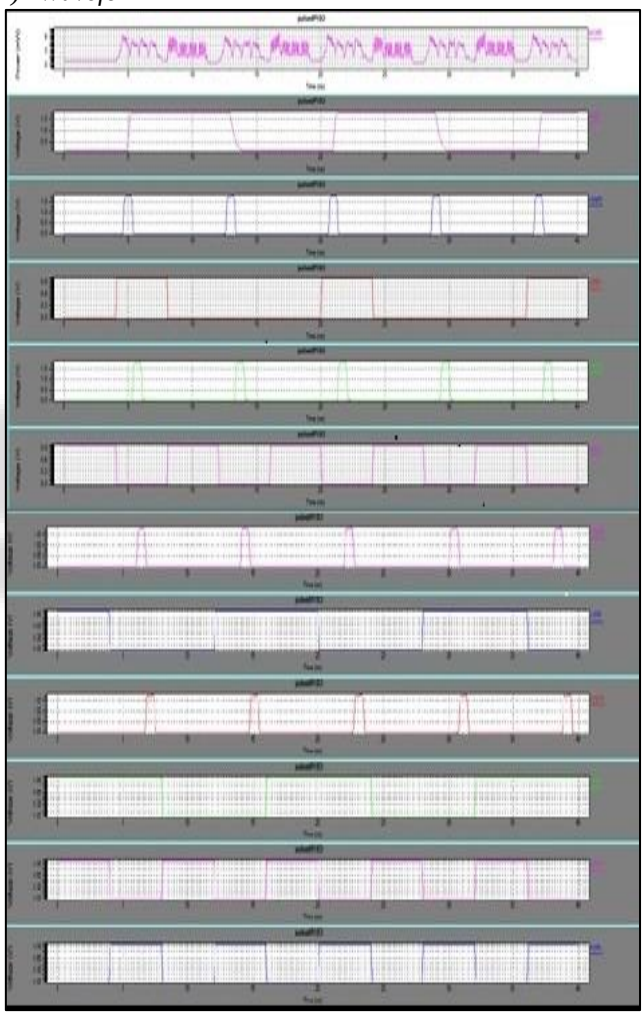

Fig. 8: Waveform of PISO using pulse latch

	PISO using pulsed latch	PISO using D flip flop
Power (uW)	293.85	552.72
Delay (ps)	29.66	43.17
Power delay product (fWs)	8.72	23.86

Table: 4 Comparison of performance parameters of PISO

D. PIPO (Parallel in Parallel out) using pulsed latch

In this implementation, the output is obtained instantly from each latch as the input is provided to each latch. Once the

latches are provided with pulse clock, input given to latch provides the output simultaneously.

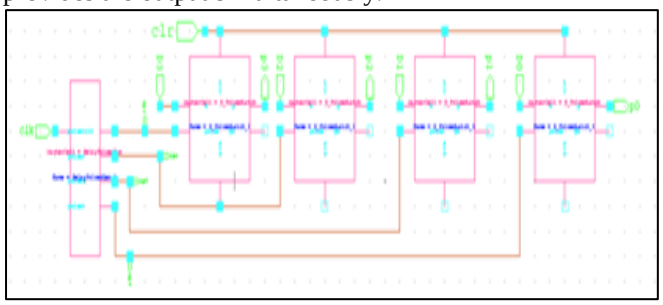

Fig. 9: Schematic of PIPO using pulse latch

1) Waveform

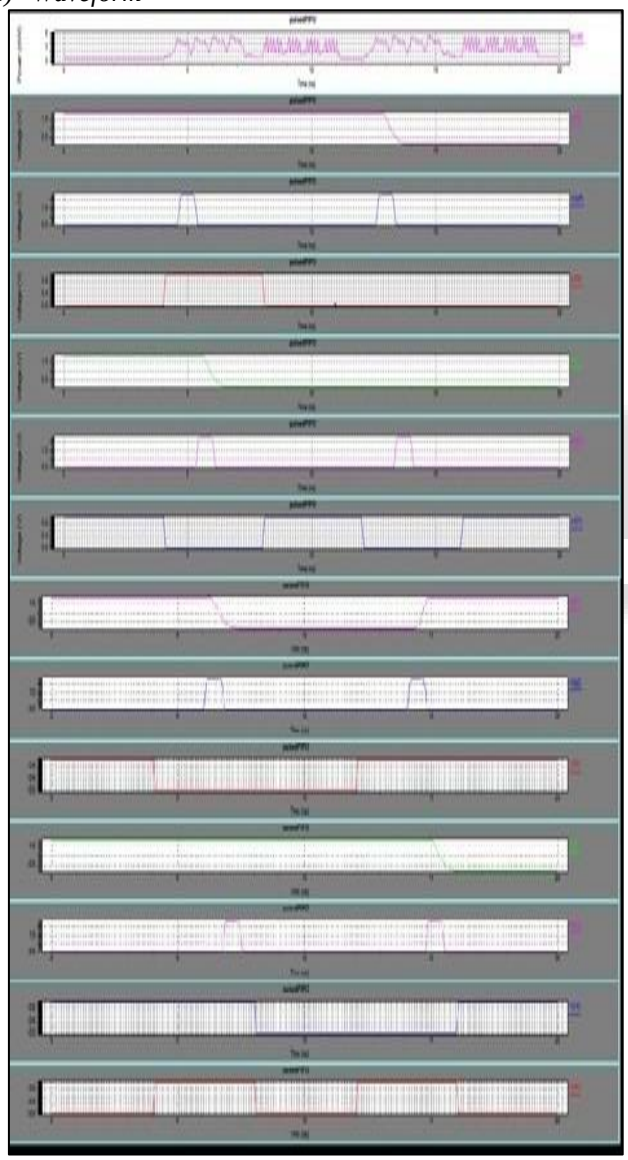

Fig. 10: Waveform of PIPO using pulse latch

	PIPO using pulsed latch	PIPO using D flip flop
Power (uW)	334.53	441.47
Delay (ps)	39.62	71.6
Power delay product (fWs)	13.25	31.61

E. Graphical Comparison of Power Consumption in Shift Registers with Flip Flop and Pulsed Latch

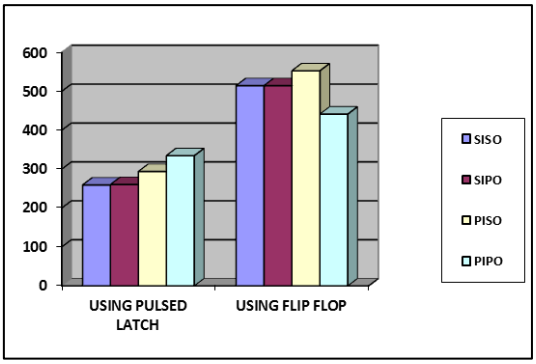

Fig. 11: Graphical comparison of power in shift registers

	% save in power	% save in power delay product
SISO using pulsed latch	49.6	72.5
SIPO using pulsed latch	49.39	61.44
PISO using pulsed latch	46.8	63.4
PIPO using pulsed latch	24.22	58.08

Table 6: Percentage save in power and power delay product

V. CONCLUSIONS

The requirement of replacement element for flip flops in recent trend, led to migration from flip flops to the pulsed latch for low power consumption, less area and delay applications. In this work, we have proposed Shift Registers and performance is compared with its conventional version. The number of transistors utilized in pulsed latch is less than that of flip flop, hence area is significantly reduced. Pulsed latch technique significantly reduces the power consumption and improves power delay product in proposed circuits.

Hence it can be inferred from the results that the pulsed latches technique can be used instead of flip flop for low power, less area, low delay and high speed applications such as mobile devices and in low power VLSI circuits.

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