Digitally Controlled PGA for Low Power Applications

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Abstract— A digitally controlled PGA with 46µW power dissipation and 1-40dB programmable voltage gain in 2dB steps is presented in this paper. It is best suited for low power applications. It has low input referred noise i.e. 2.9µV/√Hz, 3.4µV/√Hz and 1.8µV/√Hz at 1Hz, 50Hz and 200Hz respectively. The PGA has 3dB bandwidth of 20 KHz. It has PSRR that exceeds 84.5dB at all gain settings and is constant for entire 20 KHz bandwidth. In order to achieve linearity in programmable gain a new structure resistor array is proposed. The resistance is implemented by using floating active resistors which act as resistor. The advantage of floating active resistor is that they have small size and their resistance can be easily altered by changing the W/L ratios. In this work the values of floating resistor (r_{ds}) is between 180Ω-23KΩ to achieve desired gain and low power dissipation. This PGA is designed and simulated in 0.18µm technology. The simulation and layout results are obtained using Cadence's Virtuoso and Sparta tool.

Key words: PGA (Programmable Gain Amplifier), OPAMP (Operational Amplifier), EEG (Electro Encephalon Gram), ECG (Electro Cardio Gram), VGA (Variable Gain Amplifier)

I. INTRODUCTION

The PGAs are crucial components for realizing dynamic range control in low power applications. The gain control can be obtained with either digitally controlled PGAs or analog VGAs [1]. In many designs PGAs are preferred because they eliminate the use of digital to analog converter. PGA is an important conditioning block for low power applications such as bio-potential signals i.e. EEG and ECG. The voltage range of these signals is between 10µV to 10mV [2]. The PGA has three blocks i.e. gain select, resistor array and the operational amplifier. The gain control circuit adjust the output signal of the PGA to a required level which optimizes the performance of next stage. The circuit realization of PGA function can be categorized into two topologies: first is the open loop structure and second is the closed loop structure. The gain is controlled by varying the input trans-conductance or the load resistors in an open loop structure. The advantage of open loop PGA structure is that the amplifier can be designed for wide signal bandwidth. However, linearity and gain accuracy is limited by open loop structure and also, this type of structure is sensitive to the process, voltage variation and temperature. But on the other hand the closed loop PGAs can achieve more precise gain and higher linearity by using negative feedback. The gain can be realized by varying the resistance of input and feedback resistance array [3].

II. SYSTEM LEVEL DESIGN

A. Overview

This section gives a quick overview of the requirements of the design and architecture used. The key design goal is to have low power consumption for low power applications. This goal is achieved by selecting the low power consumption switches and resistor array. Also, the efforts have been made to reduce the size of differential amplifier transistors. But this results in low voltage gain of the PGA (i.e. 1-40dB). The second major requirement is the programmable gain linearity and precision, which is obtained by selecting the closed loop architecture of PGA with negative feedback. Other design specifications include CMRR>=70dB, PSRR>=80dB, low input noise, low output noise, less temperature dependence of gain and around 20KHz bandwidth. So, for this design we can use telescopic or multistage topologies of OPAMP. If pure telescopic, it will suffer from low output swing and medium gain. Therefore, we are using a two stage topology OPAMP. For digitally program the PGA a 4x16 decoder is used. The decoder is designed using CMOS AND gate, which contains NMOS and PMOS of 0.18µm technology. Floating active resistors are used in design of resistance array and NMOS is used as switch. Each floating active resistor has a different size to achieve r_{ds}.

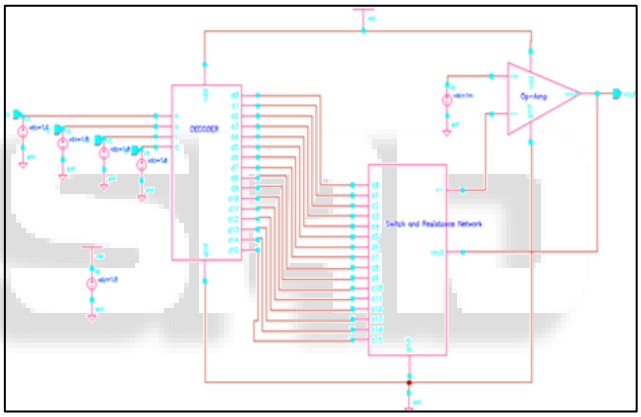

Fig. 1: Design

B. OPAMP Architecture

This architecture consists of a cascade voltage to current and current to voltage stages. The first stage consists of a differential amplifier converting the differential input voltage at transistor M1 and M2 (W=1.08µm) into differential currents. These currents are applied to a current mirror load (M3 and M4) (W=540nm, L=360nm) recovering the differential voltage. The second stage has common source MOSFET M6 (W=6.15µm, L=300nm) converting the voltage to current. This transistor is loaded by current sink load which converts the current to voltage at the output.

S. No.	Specifications	Simulation Results	Unit
1	Gain	56.9	dB
2	Phase Margin	81	Degree
3	Gain Margin	22.25	dB
4	CMRR	67.74	dB
5	PSRR	54.4	dB
6	Power Dissipation	43.94	µW
7	Input referred Noise At 0.5Hz 50Hz	 31.83 3.48	µV/√Hz

	150Hz	2.06	
8	3 dB Bandwidth	20	k Hz
9	Layout Area	0.0088	mm²
10	Slew Rate	5	V/µs
11	Unity Gain Bandwidth Product	2	MHz

Table 1: Specifications

The input differential stage is made up of p-channel transistors to reduce the flicker noise and also the overall gain is decided by this stage only. If desired for large gain we have to increase the size of M1 and M2 but it will increase the power consumption of whole system. The gain of OPAMP is given by equation (1)

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)}$$

The capacitor C_c is used for miller compensation for the stability of system. The current mirror are designed to generate a current of 10µA. Sizes of M8 and M5 are W= 380nm and L=360nm each. M9 and M10 (W=320nm, L=540nm) are used as active resistors and are directly controlled by V_{DS} and therefore channel trans-conductance becomes the channel conductance and is given by equation (2)

$$g_m = \left(\frac{\delta I_{DS}}{\delta V_{GS}}\right)(V_{DS} = constant) = \sqrt{2\beta I_D}$$

C. Resistors/ Switching Network

The schematic of resistance network is shown in figure..... Each N-MOSFET is used as a switch as well as floating active resistor. The advantage is being the small size of transistors and also low power consumption. The choice of resistor size is influenced by number of factors. Small resistor value can save area and get better noise performance. But larger resistor occupies more area and the influence of parasitic capacitor on the frequency response can be significant.

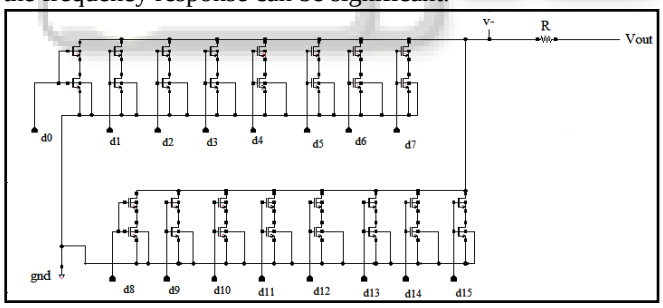

Fig. 2: Schematic of resistance network

The resistance of floating active resistance is given in equation (3)

$$r_{DS} = \frac{L}{K'W(V_{GS} - V_T)}$$

Where, L and W are length and width of n-channel MOSFET. K' is the trans-conductance parameter, V_{GS} is gate to source voltage and V_T is threshold voltage of n-channel MOSFET.

The value of r_{DS} is varied from 181Ω to 23KΩ to achieve the desired linear gain. The values of R_{ON} and R_{OFF} are set by selecting the size of W and L for each switch. The $R_{OFF}$of switch is 801MΩ for 20µ/18n i.e. W/L.

A 4-bit digital input is used to select the different gain settings ranging from 1dB to 40dB in sixteen steps. Advantage of digital control is to provide precise output to the next stage. CMOS and gates are used to implement the decoder design. The inputs are 0V and 1.8V for bit '0' and '1' respectively. The decoder outputs are connected to the gate of n-channel MOSFETs. Which is responsible to turn ON the switch. The output of decoder circuit is 1.8V and is connected to the gate of transistor switch, this will operate the transistor in saturation mode. By applying 0V the transistor can be operated in switch OFF mode i.e. cut-off mode.

III. THE OVERALL PGA BUILDING BLOCK

As shown in figure 1 the programmability of PGA is achieved by changing the input bits from 0000 to 1111 in 3dB and 2dB steps. The variable gain range is 1dB - 40dB. Due to approximated size of transistors and low tail currents the power consumption of PGA is 46µW. The differential pair of transistor of OPAMP helps in reducing the input noise of PGA. The input referred noise is tabulated below. The operating frequency of the PGA is 20KHz for each gain setting. The programmable gain is shown in figure 1. The PSRR of the PGA is achieved above 80dB and is shown in figure 2. Each gain setting have a different PSRR and all are above 80dB specification.

S. No.	Specifications	Simulation Results	Unit
1	Variable Gain Range	1-40	dB
2	Power Dissipation	46.41	µW
3	Layout Area	0.083	mm²
4	Input referred Noise At 1Hz 50Hz 200Hz	 2.93 3.45 1.80	µV/√Hz
5	Output Referred Noise at 1Hz 50Hz 200Hz	 297.2 352.9 185.1	µV/√Hz
6	3 dB Bandwidth	20	kHz

Table 2: Specifications

For PSRR measurement, a DC bias is connected to input and AC signal is connected at V_{DD} terminal and plot the graph between 20dB (V_{OUT}/V_{DD}). The layout of PGA is drawn in Cadence Virtuoso tool and layout area is 0.082mm².

IV. CONCLUSION

The design is implemented in 0.18µm CMOS process with a supply of 1.8V. The proposed low power and linear PGA architecture provides the required results. Programmable gain range of PGA is 1dB to 40dB in precise steps, it has low power consumption of 46µW. The PSRR for each step of programmable gain is above 80dB. The gain variation with the temperature is also calculated and is approximately 0.08mV/˚Cover the temperature range 0˚C - 50˚C. Table 2 compares this work with some existing representative designs, showing that the proposed design achieves low power consumption of 46µW and small chip area of 0.082mm².

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