Design and Implementation of High Speed Carry Select Adder using GDI Technique for Low Power Applications

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Abstract— Addition is a fundamental arithmetic operation usually worn in VLSI systems. The increasing demands for high speed and high resolution mixed signal integrated circuits dictate the use of Gate Diffusion Input (GDI) technique in contrast to traditional CMOS logic style. Simultaneous fulfillment of demands causes the need for the adders that has high speed and low power consumption. Solution comes to an end by the design of GDI adders. GDI is a logic style that appears to be promising in reducing power consumption, increasing speed and providing an analog and digital friendly environment. GDI technique is a novel technique which is extension of GDI (gate diffusion input) technique for low power digital circuits design further to reduce the swing degradation problem. This paper presents logic style comparisons based on different logic functions and claimed Gate Diffusion Input logic (GDI) to be much more power-efficient than complementary CMOS logic design. This technique can be used to reduce the power consumption compared to existing SQRT BK CSA using BEC, This techniques allows reduction in power consumption, carry propagation delay and transistor count of the carry select adder. Thus, the implementations of different GDI adders have been suggested in this thesis. The work shows that proposed Carry Select Adder using GDI technique has less area and consumes less power. Also it provides reduced delay comparatively and therefore can be used in various processors in order to perform fast arithmetic operations.

Key words: GDI, CMOS, BK Adder, SQRT, BEC, CSA

I. INTRODUCTION

Most of the VLSI systems, such as digital signal processing, image and video processing, and microprocessors, generally use arithmetic operations. Addition is one of the four elementary operations in mathematics, the other being subtraction, multiplication and division. In digital systems, addition forms the most important operation. This is primarily because we can perform operations like subtraction, multiplication and division using the addition operation. Hence the design of a very fast, accurate and a lower power consumption adder directly results in the increased speed of the device for faster computational purpose as well as an improved life.

Carry select adder (CSA) is one of the fastest adders having less area and power consumption. It generates partial sum and carry by considering carry input Cin=0 and Cin=1, the accurate sum and carry are selected by the multiplexers. The carry-select adder (CSA) commonly consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the estimate twice, one time with the base of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer already the correct carry is known.

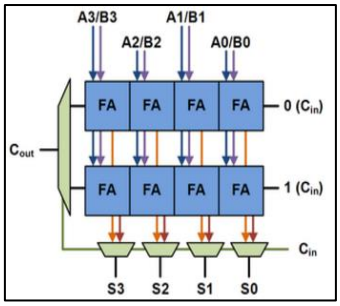

Fig. 1: Basic block diagram of carry select adder [3]

II. BASIC STRUCTURE OF GDI CELL

The GDI technique is based on the easily done cell shown in Fig.2. A fundamental GDI technique contains four terminals - G (the common gate input of the nMOS and pMOS transistors), P (the outer diffusion node of the pMOS transistor), N (the outer diffusion node of the nMOS transistor) and the D node (the commonplace diffusion of both transistors). P, N and D manage be secondhand as a substitute input or output ports, limited the circle tour structure. Table 1 shows at which point various configuration changes of the inputs P, N and G in the fundamental GDI technique become too diverse Boolean functions at the output D. GDI enables simpler gates, lessen transistor has a lot to do with, and sink power de cadence in multiple implementations, as compared with standard CMOS and Pass-transistor Logic (PTL) design techniques.

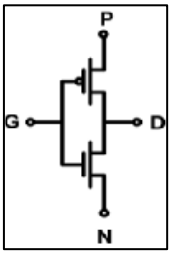

Fig. 2: Basic structure of GDI cell [11]

Most of the designed circuits were based on the F1 and F2 functions. The reasons for this are as follows.

1) Both F1 and F2 are complete logic families (allows perfection of complete accessible two-input logic function).
2) F1 is the solo GDI work that can be perfect in a standard p-well CMOS fashion, for the advantage of any nMOS is regularly and equally biased.
3) When N input is intent at an arm and a leg logic directly and P input is at peaceful logic freely, the diodes surrounded by NMOS and PMOS bulks to Out are soon polarized and there is a swiftly between N and P, procreate static a way with dissipation and Vout ~ 0.5 VDD.

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It intend be remarked that not generally told of the functions are applicable in standard p-well CMOS fashion but can be properly implemented in twin-well CMOS or silicon on insulator (SOI) technologies.

N	P	G	Out	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

Table 1: Various logic Functions implemented with GDI cell.

III. 16- BIT REGULAR SQUARE ROOT BK CSA USING BEC

Regular Square Root Brent Kung Carry Select Adder has been designed by Brent Kung adder for Cin=0 and BEC for Cin=1 and then there is a multiplexer stage. It has 5 groups of different size Brent Kung adder and Binary to Excess-l Converter (BEC). BEC is used to add 1 to the input numbers. Less number of logic gates are used to design BEC as compared to RCA herewith it consumes less area. Each group or collection contains one BK, one BEC and MUX. For N-bit Brent Kung adder, an N+1 bit BEC is used. The block diagram of the 16-bit Square Root BK Carry Select Adder using BEC is shown in Fig 3.

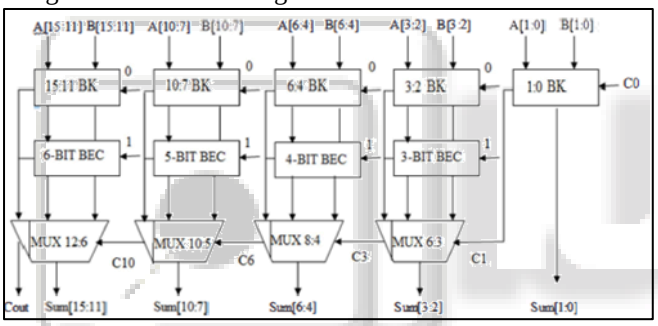

Fig. 3: 16- bit Regular Square Root BK CSA using BEC [10]

Due to the presence of different size Brent Kung adder and Binary to Excess-l Converter (BEC) & MUX, this circuit consumes large area and to reduce its area a new design of adder is used i.e. proposed 16- Bit Carry Select Adder using GDI technique.

IV. PROPOSED 16- BIT CARRY SELECT ADDER USING GDI TECHNIQUE

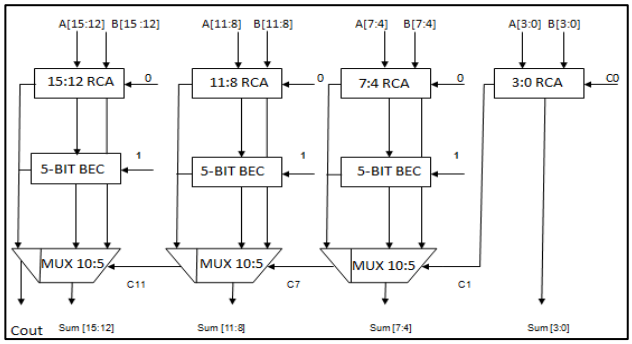

Fig. 4: Proposed 16- Bit Carry Select Adder using GDI Technique

Proposed Carry Select Adder using Gate Diffusion Input (GDI) technique has been designed. There are 4 groups. Each group contains one RCA, one BEC and one MUX. Each group has same size of RCA, Binary to Excess-l Converter (BEC) and MUX. BEC is used to add 1 to the input numbers. Less number of logic gates are used to design to Proposed 16- Bit Carry Select Adder using GDI technique as compared to regular Square Root Brent Kung Carry Select Adder using BEC therefore proposed consumes less area and power.

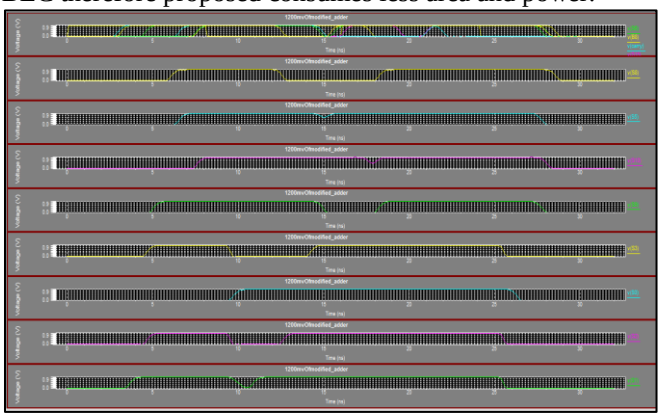

Fig. 5: Output waveform of 16- Bit Carry Select Adder using GDI Technique

V. OBSERVATION TABLE

S. No.	Name of Adder	Total No of Transistor
1	16- bit Regular Square Root BK CSA using BEC	2414
2	Proposed 16- Bit Carry Select Adder using GDI Technique	1192

Table 2: Performance Analysis Table for various 16-bit Carry Select Adder

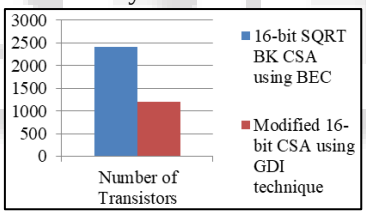

Fig. 6: Comparison of number of Transistors between Regular BK CSA using BEC and Modified CSA using GDI Technique

VI. CONCLUSION

The new implementation of GDI technique is based on the logic formulation architecture, GDI gates lower the transistor count and in turn the silicon area required when compared to standard static CMOS and dynamic CMOS based designs. The sub threshold leakage power and tunneling leakage current of GDI gates is lower than the traditional CMOS logic styles. The comparison between our analysis and prior works shows that the GDI is one of this logic styles for low power digital design does provide many advantages in VLSI systems. In short, the proposed GDI logic technique based designs can be taken a better alternative in future.

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