Analysis of Shift Register Using Flip-Flops and Pulsed Laches

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Abstract— Flip-flops and latches are the major power consuming memory element in Very Large Scale Integration digital circuits. This paper proposes a low power and delay efficient shift register using pulsed latches. The performances of memory elements are analyzed and their efficiency on power and delay are compared. The flip-flops which are chosen for comparison are explicit pulsed Data Close to output, Sense Amplifier Flip-flop, Power PC style Flip-flop and the latches which are chosen for comparison are Hybrid Latch Flip-flop, Transmission Gate Pulsed Latch and Static differential Sense Amp shared Pulse Latches .As a result of comparison, Static differential Sense Amp shared Pulse Latches is the efficient latch. So the 16 bit shift register is designed with the help of Static differential Sense Amp shared Pulsed Latches. Simulation is done using Tanner EDA tool in 180 nm technology. The power consumption is 0.23W at a 100MHz clock frequency.

Key words: Pulsed Laches, Flip-Flops

I. Introduction

Very-Large Scale integration is the process of creating an Integrated Circuit by combining thousands of transistors into a single chip. In VLSI design the high performance application such as computing, controls, telecommunications, image and video processing and consumer electronics has been rising rapidly. Sequential circuits are usually designed with flip-flops or latches which are called as memory elements. Conventional CMOS latches are built using pass transistors or tristate buffers to pass the data while the latch is transparent and feedback to hold the data while latch is opaque. It is also possible to build logic functions into the latches to reduce the sequencing overhead. Flip-flop built from a pair of back-to-back dynamic latches. Pulsed Latch is driven by even shorter pulses produced by the generator. This Pulse generator uses a fairly slow weak inverter to produce a pulse width a nominal width of about one-sixth of the cycle .When disabled, the internal node of the pulse generator floats high, but no keeper is required because the duration is short. Of course the enable signal has setup and hold requirements around the rising edge of the clock.

A shift register is a basic building block in a digital circuit. Shift registers are used in the application such as signal processing, digital filters, communication receivers and image processing Ic's etc. The area, delay and power consumption become important shift register design consideration.

II. Related Work

A. Implicit pulsed Data Close to Out Flip-flop

This flip-flop contains semi-dynamic structured and an AND logic pulsed generator. Inverters U1 and U2 are used to latch data and inverter U3 and U4 are used to hold the internal node.

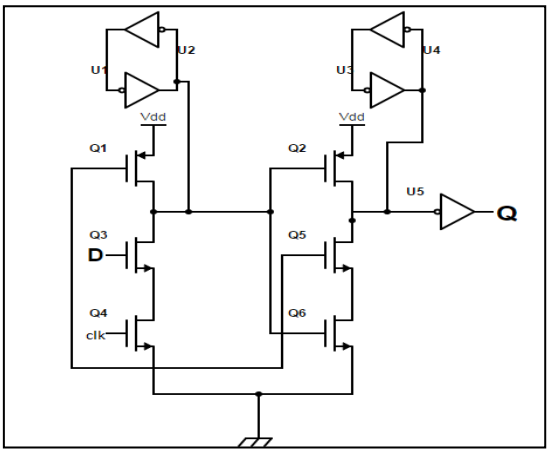

Fig. 1: Implicit pulsed Data Close to Out Flip-flop

The transistors Q4 and Q5 turn on a short period of time. During this period, the flip-flop input data is transparent to the output. After the transparent interval, the pull down paths are turn off. The delayed pulsed generator takes complimentary and skewed clock signals to produce a transparent output.

B. Sense Amplifier Flip-Flop

The sense amplifier flip-flop(SAFF)[8] contains two stages sense amplifier (SA) in the first stage and the slave set-rest (SR) latch in the second stage as shown in Fig.2. The SA stage provides a negative clock pulse on one of the inputs and SR latch captures the transition and holds the stage until the next leading clock edge arrives. SA stage is very fast but the SR latch stage doubles the delay.

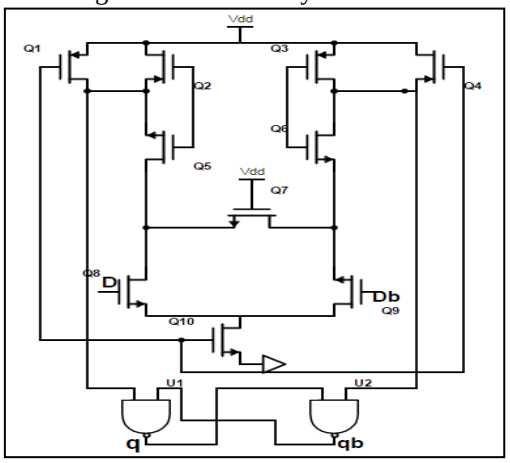

Fig. 2: sense amplifier flip-flop

C. Power PC Style Flip-Flop

The power PC style flip-flop(PPCFF)[13] is the smallest flip-flop. It contains 16 transistors. Its main advantages are the low power feedback path and short direct path. It is also having a low clock to output delay and low power dissipation. This flip-flop is constructed by cascading two pass transistor latches and provides a short clock to output delay.

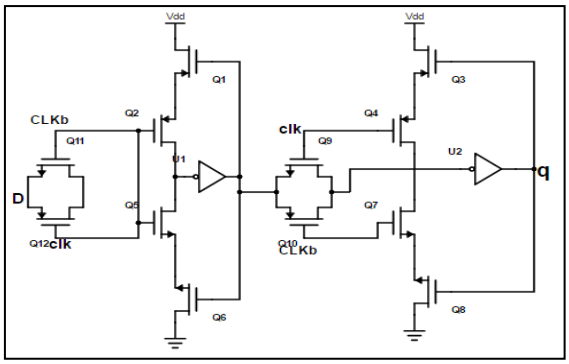

Fig. 3: Power PC Style Flip-Flop

D. Hybrid Latch Flip-Flop

The hybrid latch flip-flop(HLFF)[11] is a single-input single-output, positive edge-triggered flip-flop. At the rising edge of clock, the pull down side of both first and second stage is enabled for a period of time. During this period the flip-flop input is transparent to output. The advantage of this flip-flop is low latency, low input clock load, very small PDP and soft cycle boundary. The front end style of flip-flop is activated by a locally generated clock pulse with a static capture latch back-end.

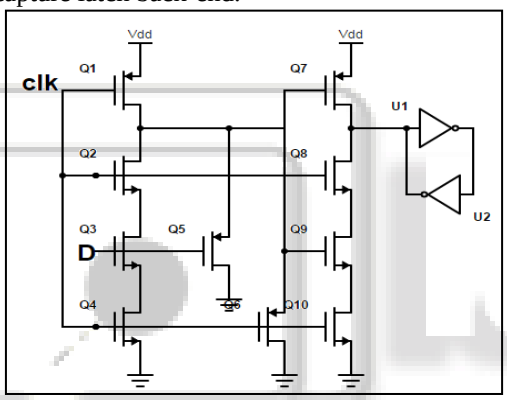

Fig. 4: Hybrid Latch Flip-Flop

E. Transmission Gate Pulsed Latch

The transmission gate flip-flop(TGPL)[9] is one of the fastest and most energy efficient in the high speed design region. It has two transmission gates that operate alternatively.

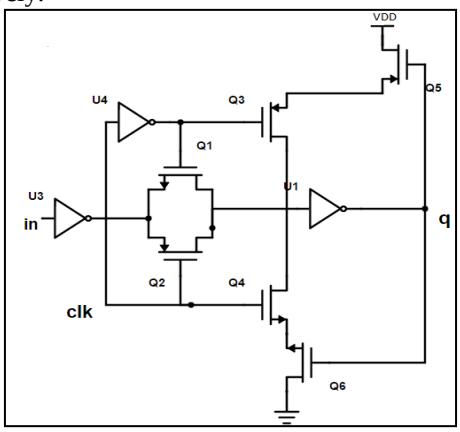

Fig. 5: Transmission Gate Pulsed Latch

When the enable falls to zero the transmission gate at the input reach cuts off and separates the input from the output. The main advantage of this latch is better hold time, clock skew hiding and pipeline overhead is reduced.

F. Static Differential Sense Amp shared Pulsed Latch

The Static differential Sense Amp shared Pulsed Latch (SSASPL)[6] is the smallest latch which consists of seven transistor. It consume low power as compare to previous latches. The SSAPL update data by three transistor Q1,Q2 and Q3 and it hold the data with two cross coupled inverters It consume lowest clock power because a single transistor driven by a clock signal.

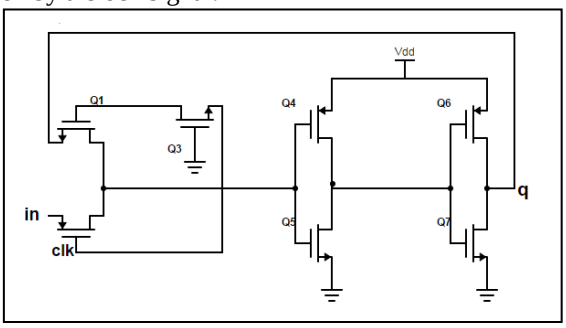

Fig. 6: Static Differential Sense Amp shared Pulsed Latch

Memory element		No. of Transistor	Clocked transistor	Power (mW)	Delay (sec)
Flip-flop	SAFF	18	3	483	99
	Ep-DCO	19	3	270	0.3m
	PPCFF	16	8	180	89µ
Latches	HLFF	14	2	270	3µ
	TGPL	10	4	231	0.3m
	SSAPL	7	1	138.6	0.8µ

Table 1: Performance Comparision Of Flip-Flop And Pulsed Latches

TABLE I shows that SSAPL consume low power and efficient delay

III. ARCHITECTURE OF SHIFT REGISTER

The shift register is classified into sub shift register[1] as shown in Fig.7 .Each Flip-flop or latches in the shift register is triggered by delayed pulsed clock generator. The non-overlapped clock signal generated with the help of delayed pulsed clock generator.

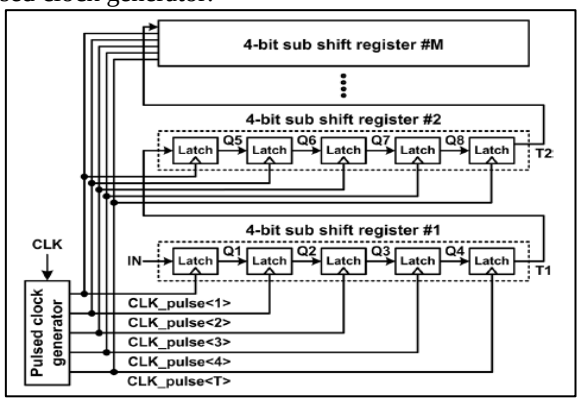

Fig. 7: Architecture of shift register

In 4-bit sub shift register, 4 latches are used to store data and 1-bit latch used for temporary storage. The latches Q1,Q2,Q3,Q4 used for data storage and data shifting and the last latch T1used for temporary storage.

The pulsed clock signal generator consists of a delay circuit and a AND gate. It able to generate a non-overlapped short clock pulse signal as shown in Fig.8.In conventional pulse generator the clock pulse width must be larger than summation of rising and falling times .In this method clock pulse width must be shorter than summation of rising and falling times.

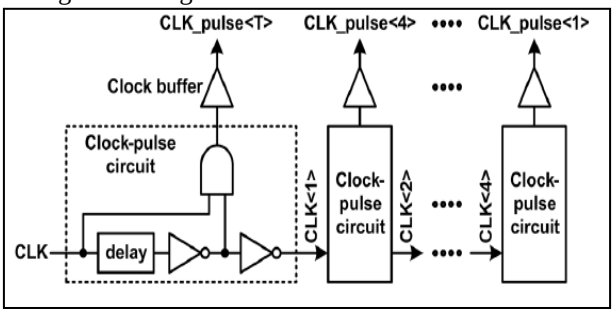

Fig. 9: Delayed pulse clock generator

IV. Result and Discussion

A 4-bit, 8-bit, 12-bit, 16-bit shift register is designed with the help of SSAPL latch which is the smallest latch consume low power and efficient delay and similarly 4-bit, 8-bit, 12-bit 16-bit shift register is designed with the help of PPCFF which is the smallest flip-flop which consume low power and efficient delay . The output of each SSAPL is connected to D input of SSAPL at its right .Grouping the register into 4 sub register and one temporary latch is used for storing the information.

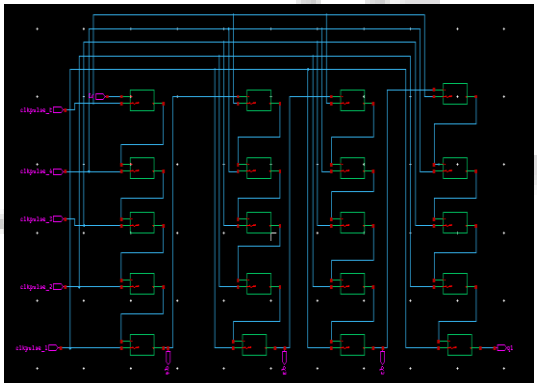

Fig. 10: Schematic of 16-bit shift register

Shift Reg.	PPCFF		SSAPL	
	Power(mw)	Delay(ms)	Power(mw)	Delay(ms)
4-bit	180	69	52	1.35
8-bit	192	71	64	1.37
12bit	223	73	77	1.39
16bit	303	120	230	70

Table 2: Performance Comparision Of Shift Register Using Ppcff And Ssapl

TABLE II shows that SSAPL shift register is efficient than PPCFF shift register because SSAPL shift register consume low power and efficient delay.

V. Conclusion

A low power and delay-efficient 4-bit,8-bit,12-bit, 16 bit shift register was designed with the help of Static differential Sense Amp shared Pulsed Latches (SSASPL) and Power PC flip-flop(PPCFF). The area and power consumption are reduced by replacing flip-flops with pulsed latches.. The shift register uses a small number of the pulsed clock signals and classified the latches into sub shift registers and also additional temporary storage latches are used. A 16-bit shift register using pulsed latches was designed using a 0.18µm CMOS process with V_{DD}=1.8V. The power consumption is 0.23W at a 100 MHz clock frequency. Thus shift register saves power as compared to the conventional shift register.

VI. Future Work

The shift register using SSASPL latch is implemented in the application of LFSR counter. An N-bit linear-feedback shift registers sequences through up to 2^N-1 outputs in pseudo-random order. It has a short minimum cycle time independent of N , so it is useful for extremely fast counter as well as pseudo-random number generation. The pseudo-random sequences are widely used for built-in self-test and bit-error-rate testing in communications links. They are also used in many spread-spectrum communications systems such as GPS and CDMA.

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