Analysis of the Effect of Temperature and Supply Voltage Variations on Leakage Power in Conventional 6T-SRAM Cell at Different Process Corners

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Abstract— In deep-submicron processes, Leakage power becomes critical factor. In recent technologies, leakage power is a major concern, as it impacts battery lifetime. When memory cell runs in standby mode, power dissipation occurs. Due to maximize power dissipation, battery life decreases in portable devices. In this paper, we have performed simulation and analysis of a conventional 6T SRAM Bit-cell thereafter a comparative analysis is being performed for the leakage power at 45nm and 32nm CMOS technology at different process corners using HSPICE circuit simulator. Effect of temperature and voltage variations on leakage power are also explored in this paper to create effect as a practical environment. When we kept VDD=1v, 45nm based 6T SRAM cell gives 50.27% minimum leakage power at SS corner as compare to 32nm based 6T SRAM cell significantly.

Key words: Conventional 6T SRAM Cell, Process Corners, DIBL, Sub-Threshold Leakage and Leakage Power

I. INTRODUCTION

Low power Requirement is essential in portable electronic devices to maximize the battery lifetime [1]. Continuous scaling of CMOS devices results high packaging density but increases the importance of power even more noticeable in portable semiconductor applications. In integrated circuits, supply voltage is scaled down for suppressing power consumption[2] . For achieving low-power operation, power supply scaling is one the most common and able approach [3]. In this paper we have analyzed the Leakage power of the 6T SRAM cell at SS, FF, TT, FS, SF corners. After that we have described which process corner is dominant for the minimum leakage power as compare to the other process corners. We have also discussed which technology node is suitable for minimum power consumption. Lowering the supply voltage (V_{DD}) and temperature are a promising way to reduce power consumption.

This paper is organized as follows, Section II discussed about conventional 6T SRAM cell. Section III includes power dissipation. Section IV has discussed the process corner analysis and after this in section V, we have discussed about the standby leakage power of conventional 6T SRAM at various CMOS technologies.

II. CONVENTIONAL 6T SRAM CELL

The standard 6T SRAM cell shown in Fig.1 that uses two cross coupled inverters act as a latch circuit and two access transistors. In the latch circuit, two inverters are connected back to back; In a SRAM cell, each bit is stored on four transistors (M3, M4, M5, and M6). The read and write operations in 6T SRAM cell is done by two additional access transistors .These two access transistors are enabled, when word line (WL) is asserted high. When the word line is high BL and BLB lines are connected to the latch circuit to transfer the data for both read and write operations [4]. The standard 6T SRAM cell operates in three modes:

A. Hold Operation

If the word line is low (WL=0), the access transistors disconnect SRAM cell from BL and BLB. In this operation, SRAM cell is capable to retain the data as long as it is powered.

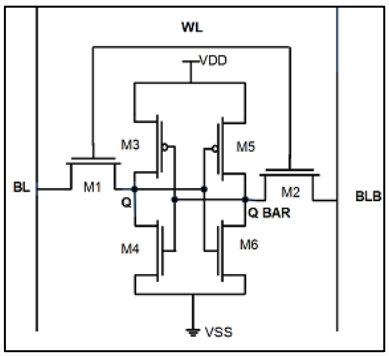

Fig. 1: Conventional 6T SRAM Cell

B. Write Operation

In this operation, SRAM cell can be written with different bit value replacing its originally stored bit. When word line is high (WL=1) our access transistors (M1 and M2) are activated to perform the write operation. That means if we want to written required data ('1') to the SRAM cell, We must provide data(1) to bit line and its complement(0) to the bit line bar This operation would make the 6T SRAM cell to change its state according to this arrangement.

C. Read Operation

In this operation, SRAM cell is capable to communicate its stored data to the bit-lines. This mode of operation does not affect the data. To read the data from the SRAM cell, first the WL is asserted high ('1') which activates the access transistors to access the latch circuit. To perform read operation, both the bit lines like BL and BLB are pre-charged to V_{DD} value. During read operation, current flows from the one bit line to the ground through the access transistor. Due to which one of the bit lines discharged to ground and other would remain pre-charged to supply voltage or vice versa.

III. POWER DISSIPATION

Leakage power is primarily the result of unwanted sub-threshold current in the transistor channel when the transistor is turned off. When the input voltage at the gate terminal with respect to source is less than the threshold voltage (Vth), current flows through MOSFET from power supply to ground is called as Sub-threshold current[5].

When the CMOS 6T SRAM cell operates in hold mode, There is small current flowing through the power supply to the ground is called leakage current of the 6T

SRAM cell[6]. Due to which leakage power dissipation occurs in the memory cell. Leakage power dissipation can be described as follows:

P_{total} = Total Leakage Current × Supply Voltage (V_{DD})

IV. PROCESS CORNER ANALYSIS

The collective effects of process and environmental variation can be lumped into their effect on transistor: typical (also called nominal), fast or slow. When these processing variations are combined with the environmental variations, we 'define design or process corners. The term corner' refers to an imaginary box that surrounds the guaranteed performance of the circuits. A process corner is an example of a design-of-experiments (DoE) technique that refers to a variation of fabrication parameters used in applying an integrated circuit design to a semiconductor wafer[7]. The first three corners (TT, FF, SS) are called even corners, because both types of devices are affected evenly, and generally do not adversely affect the logical correctness of the circuit. The resulting devices can function at slower or faster clock frequencies, and are often binned as such. The last two corners (FS, SF) are called "skewed" corners, and are cause for concern. This is because one type of FET will switch much faster than the other, and this form of imbalanced switching can cause one edge of the output to have much less slew than the other edge.

V. SIMULATION AND RESULT

Leakage power occurring when device is in hold mode of the 6T SRAM cell. We have analyzed effect of leakage power at different process corners, voltages and temperatures at different technology

– Effect of voltage (V_{DD}) on leakage power From the Fig.2, We can observe that if we increase the V_{DD}, leakage power also increases. This is because, when applied high drain voltage is increased at the drain terminal of short-channel devices, and then the barrier height is lowered resulting in shifting toward the source end. This phenomenon is called a DIBL (drain-induced barrier lowering). Due to this phenomenon threshold voltage (V_{th}) of the MOSFET decreases to maintain high drive current[8]. We can see that minimum leakage power observed in case of SS corner and the maximum leakage power observed at FF corner at 45nm technology. When we kept V_{DD} at 0.6v, leakage power 94.05% reduced at SS corner as compare to the FF corner as shown in Table 1. When we kept V_{DD}= 1v, leakage power 96.90% reduced at SS corner as shown in Table I.

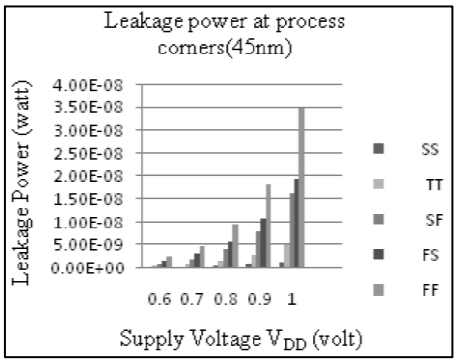

Fig. 2: Leakage Power Vs voltage variation at different process corners at 45nm.

V_{DD} (volt)	SS	TT	SF	FS	FF
0.6	1.45 E-10	5.06E-10	9.32E-10	1.65E-09	2.44E-09
0.7	2.44E-10	9.22E-10	1.96E-09	3.17E-09	4.88E-09
0.8	4.04E-10	1.65E-09	4.02E-09	5.92E-09	9.54E-09
0.9	6.62E-10	2.89E-09	8.16E-09	1.08E-08	1.83E-08
1	1.08E-09	5.05E-09	1.65E-08	1.95E-08	3.49E-08

Table 1: Leakage power (watt) at various V_{DD} for 6T SRAM cell at 45nm at 25°C

From the Fig.3, We can see that minimum leakage power observed in case of SS corner and the maximum leakage power observed at FF corner at 32nm technology. When we kept V_{DD} at 0.6v, Leakage power 96.24% reduced at SS corner as compare to the FF corner as shown in Table II When we kept V_{DD}= 1v, leakage power 98.60% reduced at SS corner as shown in Table II.

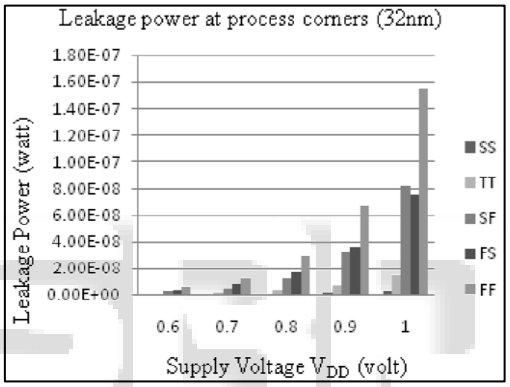

Fig. 3: Leakage power Vs voltage variation at different process corners at32nm

V_{DD} (volt)	SS	TT	SF	FS	FF
0.6	1.93E-10	8.42E-10	1.92E-09	3.41E-09	5.14E-09
0.7	3.60E-10	1.77E-09	4.95E-09	7.67E-09	1.23E-08
0.8	6.58E-10	3.65E-09	1.25E-08	1.68E-08	2.87E-08
0.9	1.19E-09	7.48E-09	3.18E-08	3.58E-08	6.64E-08
1	2.15E-09	1.54E-08	8.16E-08	7.48E-08	1.54E-07

Table 2: Leakage power (watt) at various V_{DD} for 6T SRAM bitcell at 32nm at 25°C

According to both results, 45nm 6T SRAM bitcell gives minimum leakage power as compared to the 32nm 6T SRAM bitcell in the case of voltage variation.

– Effect of temperature on leakage power: The simulation is done to analyze the effect of different temperatures on leakage power at different process corners as shown in fig. 4-5. From Fig.4 and Fig.5, it is found that the leakage power increases with increase in temperature. In case of temperature variation, we can see that the minimum leakage power observed at the SS corner and the maximum leakage power observed at the FF corner at 45 nm technology. When we kept Temperature at 25°C,

leakage power 92.54%% reduced at SS corner as compare to the FF corner as shown in Table III. When we kept Temperature at 100°C, leakage power 89.33% reduced at SS corner as shown in Table III.

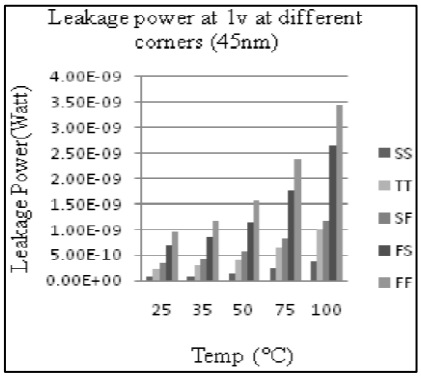

Fig. 4: Leakage power Vs Temperature variation at different process corner at 45nm

Temp(°C)	SS	TT	SF	FS	FF
25	7.07E-11	2.22E-10	3.42E-10	6.77E-10	9.48E-10
35	9.15E-11	2.82E-10	4.14E-10	8.42E-10	1.16E-09
50	1.31E-10	3.94E-10	5.43E-10	1.14E-09	1.55E-09
75	2.27E-10	6.48E-10	8.17E-10	1.79E-09	2.38E-09
100	3.68E-10	1.00E-09	1.17E-09	2.64E-09	3.45E-09

Table 3: Leakage power (watt) at various temperature for 6T SRAM bitcell at 45nm

And at 32 nm technology, that the minimum leakage power observed at the SS corner and the maximum leakage power observed at the FF corner. From fig.4 and fig.5, when we kept temperature at 25°C, leakage power 94.784% reduced at SS corner as compare to the FF corner as shown in Table IV. When we kept temperature at 100°C, leakage power 92.15% reduced at SS corner as shown in Table IV.

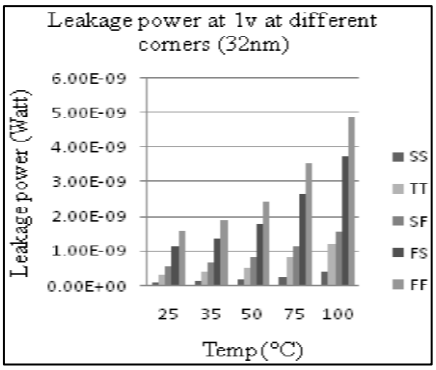

Fig. 5: Leakage power Vs Temperature variation at different process corner at 32nm

Temp(°C)	SS	TT	SF	FS	FF
25	8.24E-11	3.07E-10	5.40E-10	1.12E-09	1.58E-09
35	1.05E-10	3.81E-10	6.35E-10	1.36E-09	1.89E-09
50	1.47E-10	5.17E-10	7.98E-10	1.78E-09	2.43E-09
75	2.44E-10	8.13E-10	1.13E-09	2.65E-09	3.53E-09
100	3.83E-10	1.21E-09	1.53E-09	3.74E-09	4.88-09

Table 4: Leakage power (watt) at various temperature for 6T SRAM bitcell at 32nm

We observed that 45 nm 6T SRAM bit cell gives minimum leakage power as compared to the 32nm technology in the case of temperature variation.

VI. Conclusion

In this paper, we have analyzed the 6T SRAM bit cell at different technologies. The cell has been analyzed at various process corners to check the leakage power at 45nm and 32nm technology. On analyzing the various corners, we found that the minimum leakage power at SS corner as compared to other corners at 45nm and 32nm technologies in the case of voltage and temperature variations. We have also found that as the voltages and temperatures reduced, the leakage power also reduced.

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