Frequency Analysis of different configurations of Current Starved Voltage controlled oscillators using 180nm CMOS Technology

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Abstract— In this paper multiple stage of CSVCO are studied and simulated. The design is implemented in Ngspice V21 with high oscillation and Supply voltage VDD of 2V.Tuning range and Oscillation frequency of different stages of CSVCO is achieved. The circuit is simulated using 180nm model. Simulation result proved that wide range of oscillation can be achieved using three stages CSVCO where higher stability and noise margins are achieved in more than three-stage VCO. Design procedures and simulation Results are illustrated.

Key words: Current Starved Voltage Controlled Oscillator, Complementary Metal Oxide Semiconductor, Ngspice, Origin

I. INTRODUCTION

A CMOS VCO (Voltage Controlled Oscillator) is an important block of PLL (Phase Locked Loop) and also it has multiple applications in digital as well as analog communication. The power consumption and the area occupied by a PLL is mainly depend on VCO. Thus VCO should be of less area and low power consumption as well. This proposed design methodology consumes minimum phase noise due to novel infeasibility driven evolutionary algorithm (IDEA). VCO is an important component of Radio Frequency transceivers and it is commonly used in various tasks of signal processing such as selection of frequency and generation of signal. These days Radio Frequency transceivers also constitute of PCF (Programmable Carrier Frequencies) and thus they also rely on PLL. The transceivers of wireless communication system comprises of PA (Power Amplifiers), LNA (Low Noise Amplifiers), DSP(Digital Signal Processing) chip.

II. CURRENT STARVED VCO

A. CSVCO Overview

Basic Architecture of CSVCO is shown in Fig. 1. CSVCO works as a ring oscillator similarly. It is observed that MOSFETs M2 and M3 operate as an inverter, while MOSFETs M1 and M4 operate as current sources. The current sources, M1 and M4, limit the current available to the inverter, M2 and M3; in other words, the inverter is starved for the current. The MOSFETs M5 and M6 drain currents are the same and are set by input control voltage, which is varied in the steps of 0.5V, starting with 5V. The currents in M5 and M6 are mirrored in each inverter/current source stage.

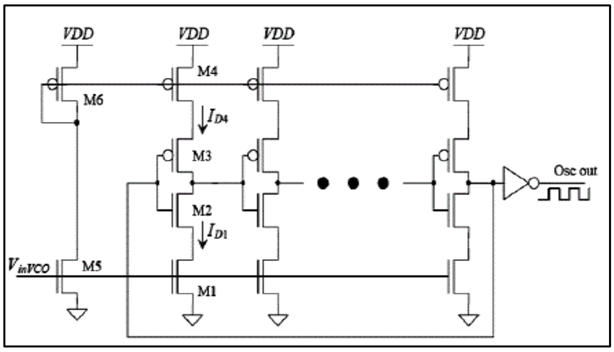

Fig. 1: Basic architecture of CSVCO

The Output Frequency of CSVCO can be calculated by the following equations:

The total capacitance on the drains of M2 and M3 is given by

$$C_{total}=C_{out}+C_{in} \quad (1)$$

Where the output capacitance is given by

$$C_{out} = C_{ox}(W_pL_p+W_nL_n) \quad (2)$$

The input capacitance is given by

$$C_{in}=(3/2)C'_{ox}(W_pL_p+W_nL_n) \quad (3)$$

So the Total Capacitance is,

$$C_{total}= (5/2)C'_{ox}(W_PL_P+W_nL_n) \quad (4)$$

If t_1 is the time for $C_{total}$for charging from Zero

$$t_1=C_{total}\ V_{SP} *1/\ I_{D4} (5)$$

and t_2 is the time for C_{total} for discharging fromV_{DD} to V_{SP},

$$t_2=C_{total(}V_{DD}-\ V_{SP)}*1/\ I_{D1} (6)$$

If we set ID4= ID1= ID (which will ID centre when Vin VCO = $V_{DD}/2$), then the sum of t1 and t2 is simply

$$t_1+t_2 = (C_{total}\ V_{DD)\ *}\ 1/I_D (7)$$

The oscillation frequency of the current-starved VCO for N (an odd number > 3) stages is

$$f_{osc} = 1/N\ (t_1+t_2)= I_D/\ N\ C_{total}V_{DD} (8)$$

Which is equal to f_{center} (at V_{in}VCO = $V_{DD}/2$ and I_D = $I_D$center).

Which is equal to f_{center} (at V_{in}VCO = $V_{DD}/2$ and I_D = $I_D$center). The VCO stops oscillating, when V_{in}VCO< $V_{TN.}$ Therefore, we can define V_{min}= V_{TN} and f_{min}= 0. The maximum VCO oscillation frequency, $f_{max}$is determined by finding ID when V_{in}VCO=V_{DD}. At the maximum frequency, V_{max}= $V_{DD.}$We can form different stages of CSVCO which should be always in Odd numbers for the purpose of Oscillation.

B. Three Stages Csvco

The three stageCSVCO Shown in Fig 2 has been realized by NG Spice tool. The table1shown below depicts the different frequency ranges for the different control Voltages. Here we get Oscillation between 570.9 MHZ to 3417.8 MHZ for the control voltages lies between 0.6 V to 2 V. As the Voltage increases the frequency also increases linearly.

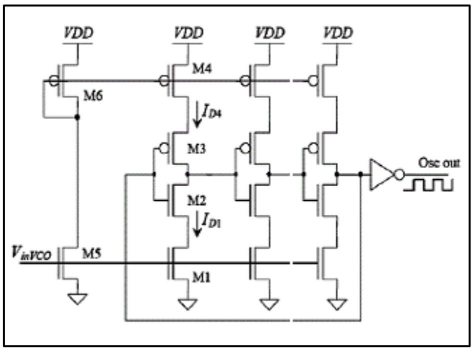

Fig. 2: Three Stages CSVCO

Control Voltage	Frequency (MHZ)
0.6	570.9
0.7	1236.3
0.8	2341.8
0.9	2349.3
1	2691.7
1.1	2920.3
1.2	3064.1
1.3	3157.9
1.4	3163.4
1.5	3183.3
1.6	3256.1
1.7	3349.7
1.8	3372.9
1.9	3391.7
2	3417.8

Table1: Voltage Control and Frequency of CSVCO3

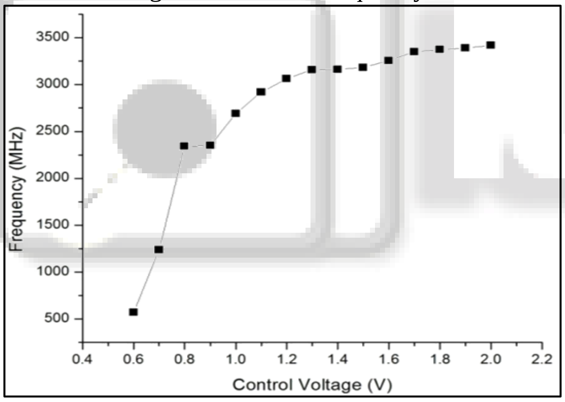

Fig. 3: Curve of CSVCO3

C. Five Stages Csvco

The Five stages CSVCO Shown in Fig 4 has been realized by NG Spice tool. The table shown below depicts the different frequency ranges for the different control Voltages. Here we get Oscillation between 345 MHZ to 2392.7 MHZ for the control voltages lies between 0.6 V to 2 V. As the Voltage increases the frequency also increases linearly.

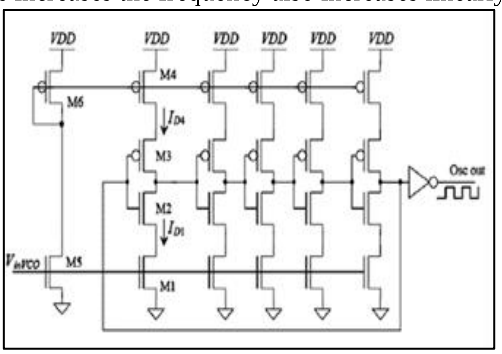

Fig. 4: Five Stages CSVCO

Control Voltage	Frequency (MHZ)
0.6	345
0.7	727.9
0.8	1067.6
0.9	1361.4
1	1554
1.1	1759.6
1.2	1777.3
1.3	1832.2
1.4	1869.7
1.5	1886.1
1.6	1937.9
1.7	1985.3
1.8	1987.1
1.9	2116.4

Table 2: Voltage Control and Frequency of CSVCO5

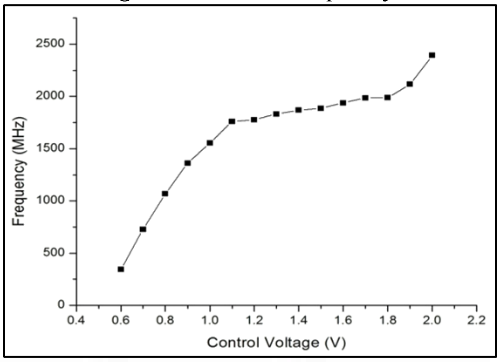

Fig. 5: Curve of CSVCO5

D. Seven Stages Csvco

The CMOS circuit of seven stages CSVCO Shown in Fig 6 has been realized by Ngspice tool. The table shown below depicts the different frequency ranges for the different control Voltages. Here we get Oscillation between 312.7 MHZ to 1424.4 MHZ for the control voltages lies between 0.6 V to 2 V. As the Voltage increases the frequency also increases linearly.

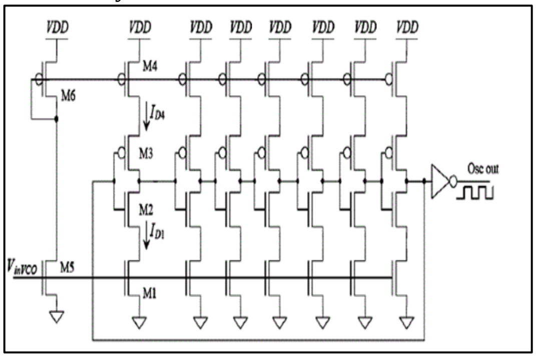

Fig. 6: Seven Stages CSVCO

Control Voltage	Frequency (MHZ)
0.6	312.7
0.7	537.9
0.8	794.3
0.9	994.4
1	1021.1
1.1	1230.2
1. 2	1306.1
1.3	1330.3
1.4	1372.8
1.5	1375.7

1.6	1388
1.7	1401.3
1.8	1403.4
1.9	1404
2	1424.4

Table 3: Voltage Control and Frequency of CSVCO7

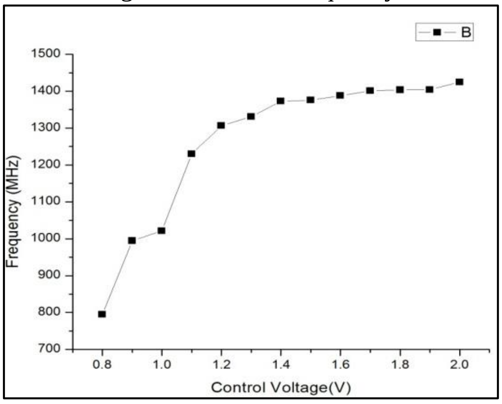

Fig. 7: Curve of CSVCO7

Parameters	Three Stages	Five Stages	Seven Stages
Technology	180 nm	180 nm	180 nm
Supply Voltage	2V	2V	2V
Frequency Range	570.9 MHz to 3417.8 MHz	345 MHz to 2392.7 MHz	312.7 MHz to 1424.4 MHz
Starting Oscillation Frequency	570.9 MHz	345 MHz	312.7 MHz
Control Voltages Range	0.6V to 2V	0.6V to 2V	0.6V to 2V

Table 4:

III. CONCLUSION

Various stages of CSVCO have been studied and implemented in 180nm submicron technology using NGspice circuit simulator tool also corresponding graphs of respective stages are carried out using Origin version 8.0. It has been observed that, wide range of oscillation can be achieved using 3 stage CSVCO configurations but at the same time noise margin is very poorer in CSVCO3. Which can be further improved with the help of CSVCO7.

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