# Analysis and Design of Multi level Inverter

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*Abstract*— Multilevel Inverter (MLI) has been accepted as an attractive topology for high voltage DC-AC conversion. This paper focuses on a reference modulation technique for a hybrid multilevel inverter technique based on reduced Total harmonic distortion and total number of used Power electronics Switches the results of reduction of total cost ,installation area and reduced circuit complexity due to gate driver circuit. Pulse width modulation technique to generate firing pluses. Over all circuit present higher number of level with use of less number of powers switches. Simulation and THD results show with MATLAB/SIMULINK platform.

***Key words:*** Symmetrical multilevel Inverter, Bidirectional switch, Total Harmonic Distortion (THD)

## I. INTRODUCTION

Increasing demand of power, forced to choose renewal energy option for fulfillment of requirement of power, The role of power electronics converters in modern power systems is becoming even more Prominent, A multilevel inverter (MLI) is a power electronic converter built to synthesize a desired AC voltage from several levels of different DC voltages which the DC levels were considered to be identical in that all of them were batteries, capacitors, solar cells, etc. The multilevel inverter has gained much consider in recent Years due to its advantages in lower devices switching loss better higher voltage capability, electromagnetic compatibility, and lower harmonics [1]-[3]. Several topologies for multilevel inverters have been presented; the most popular being the diode-clamped (DC-MLI) [4], [5], flying capacitor [6], and cascade H bridge (CH-MLI) [7] structures. Besides the three basic multilevel inverter (MLI) topologies; other multilevel converter methodology have been presented, most of these are hybrid circuits that are combinations of two of the basic multilevel methodology.

There most acceptable and continuously research on Cascaded Hybrid multilevel inverter, The recent applications of MLI's have a variety including motor drives and induction machine, active rectifiers, filters, flexible AC transmission systems (FACTS), interface of renewable energy sources, and static compensators. The diode clamped inverters (DC-MLI), particularly the three-level multi level structure, have a wide popularity in motor drive applications besides other multilevel inverter topologies. However, it would be a extent of complexity and number of clamping diodes for the DC-MLIs, when the level exceeds three [9-10]. The flying capacitor multi level inverter (FC-MLIs) is based on balancing capacitors on phase buses and generates multilevel DC output voltage waveform clamped by capacitors instead of diodes. The FC-MLI topology also requires balancing capacitors per phase at a number of (m-1) *(m-2)/2 for an m-level inverter(MLI) and it will cause to higher the number of required capacitor in high level inverter methodologies and complexity of considering DC-link voltage balancing.

## II. TOPOLOGY AND ITS WORKING

### A. Structure

This paper presents a fully control hybrid multi level inverter with twelve IGBT power electronics switches and four DC voltages it helps to generate 9-level voltage.

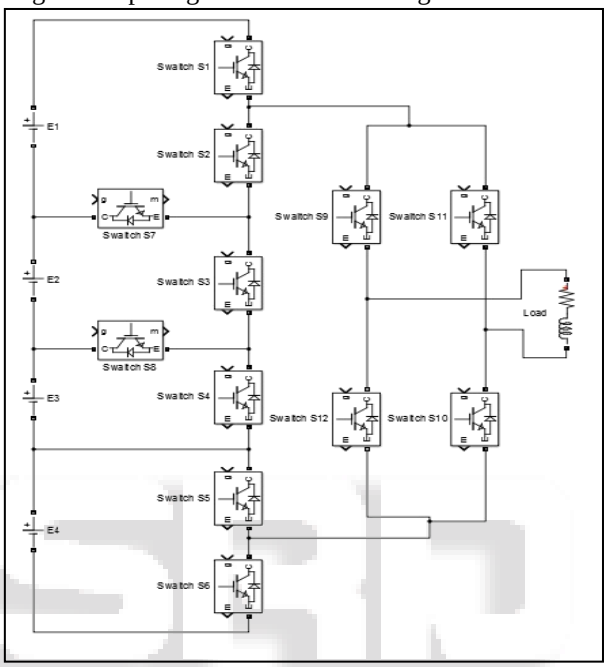



Fig. 1: Circuit Diagram of 9- Level Inverter

| System Parameters | Value | | | |
|---|---|---|---|---|
| Reference frequency | 50 Hz | | | |
| Carrier frequency | 1500 Hz | | | |
| Load resistance | 1Ω | | | |
| Load inductance | 3 mh | | | |
| DC Source | $E_1$=100v | $E_2$=100v | $E_3$=100v | $E_4$=100v |

Table 1: System Parameters

### B. Working

## III. SWITCHING SCHEME SIMULATION RESULTS

Recurrently three major PWM techniques are used in multilevel inverters: (1) sinusoidal PWM (SPWM), (2) third harmonic injection PWM (THPWM), and (3) space vector PWM (SVM), had reported about multicarrier based PWM techniques. To be specific, sinusoidal carrier based PWM approaches are quite good to handle; level shift Pulse Width M technology is used in this paper sinusoidal wave taken as reference wave and deferent triangular pulse modulation e is used as carrier wave after use of comparator produces aggregated signal as shown in **fig.3,** this aggregated signal

produces firing pulses for different twelve power electronics switches.

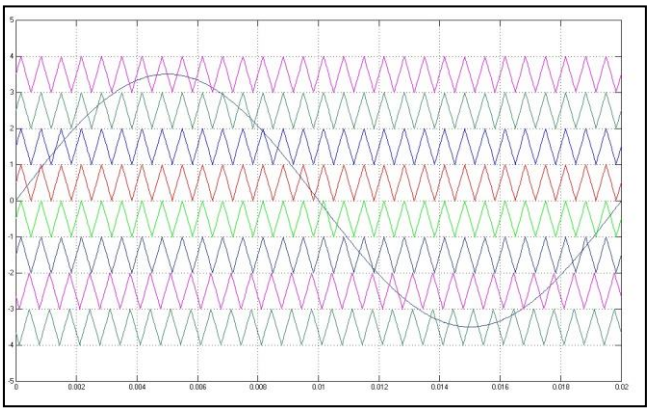


Fig. 2: PWM Firing Scheme

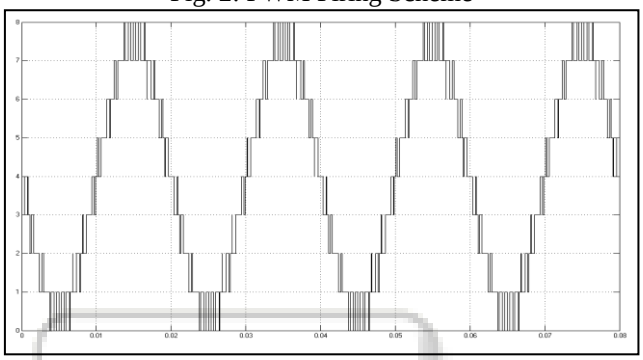


Fig. 3: Aggregated Signal

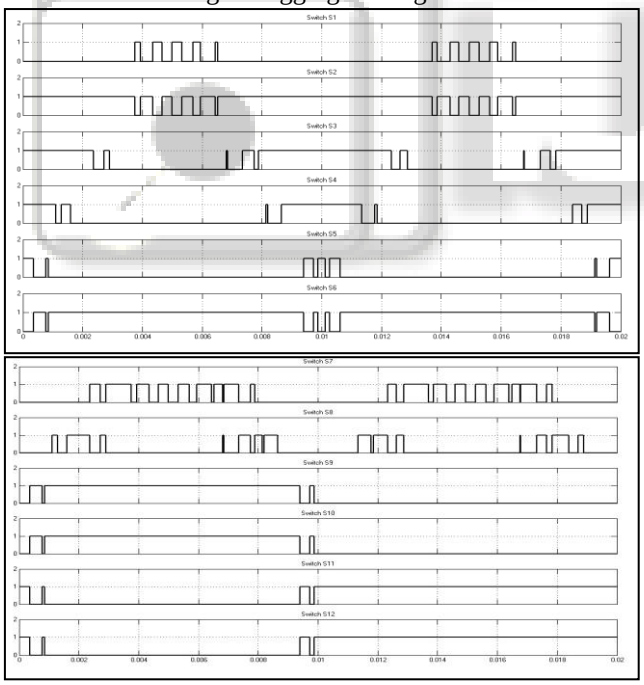
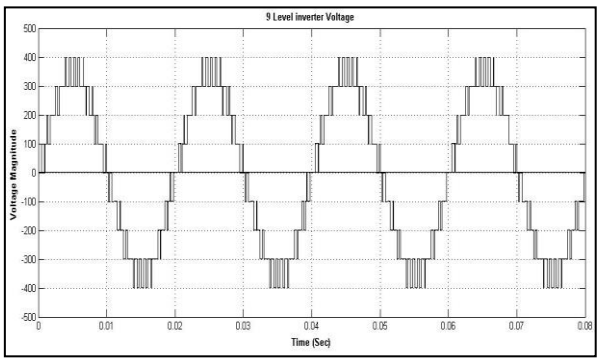



Fig. 4: Gate Firing Pulses

## IV. SIMULATION RESULTS



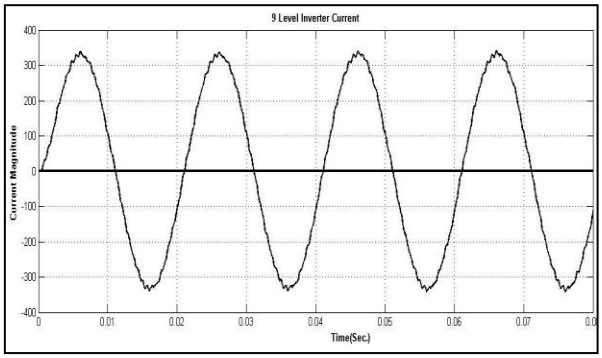
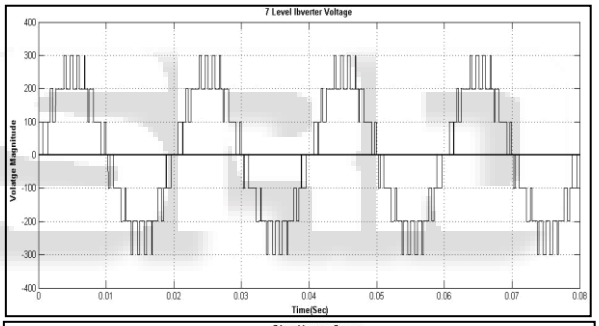




Fig. 5: (a) 9-level inverter voltage (b) 9-level Inverter current



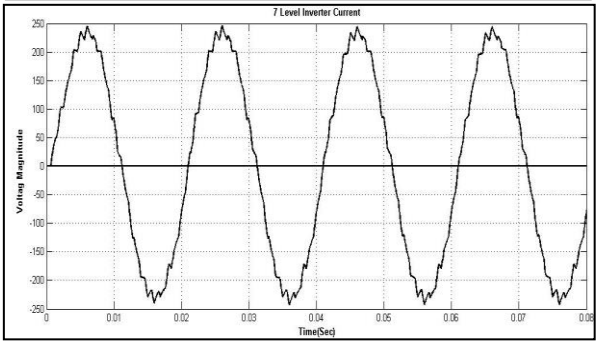




Fig. 5: (a) 7-level inverter voltage (b) 7-level Inverter current

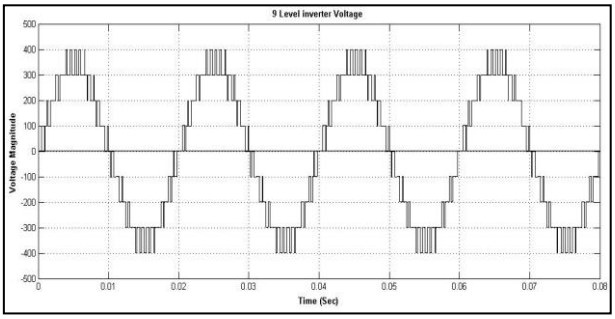



Fig. 6: 9-Level Voltage THD

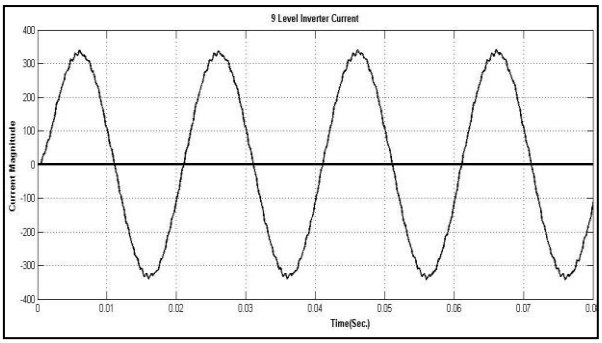



Fig. 7: 9-Level Current THD

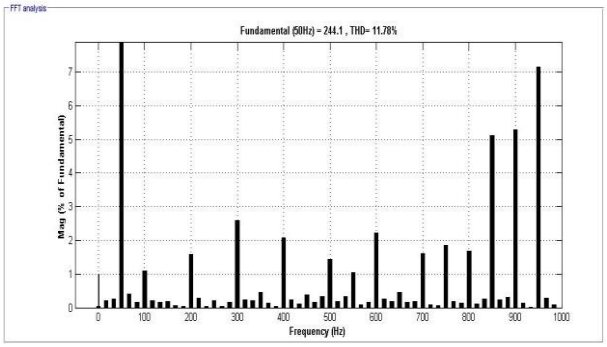



Fig. 8: 7-Level Voltage THD

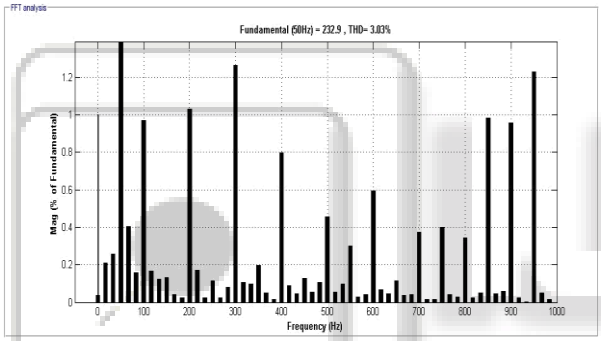



Fig. 9: 7-Level Current THD

## V. COMPARATIVE STUDY

Typical present topology has several disadvantages over present topology as higher number of diode and capacitors used, this increase over all circuit cost and space required, and cascaded hybrid multi level inverter has used higher number of power electronics switches due to which system complexity increase even THD ratio increase with the increases of power electronics switches. Overall results discussed as shown in table as listed below.

| Inverter | Fundamental voltage[V] | | | | Frequency [Hz] | Voltage (THD) % | Current (THD) % |
|---|---|---|---|---|---|---|---|
| | $E_1$ | $E_2$ | $E_3$ | $E_4$ | | | |
| 7-level Inverter | 100v | 100v | 100 | NO | 50 | 12.35 % | 1.12 % |
| 9-level Inverter | 100v | 100v | 100v | 100v | 50 | 4.27 % | 0.77 % |

Table 2: Comparison between Different Levels.

| Inverter Configuration | Diode-Clamp | Flying-Capacitors | Cascaded inverters | New MLI |
|---|---|---|---|---|
| Switching devices | 2(m-1) | 2(m-1) | 2(m-1) | M+3 |
| Main diodes | 2(m-1) | 2(m-1) | 2(m-1) | 0 |
| Clamping diodes | (m-1)(m-1) | 0 | 0 | 0 |
| DC bus capacitors | (m-1) | (m-1) | (m-1)/2 | 0 |
| Balancing capacitors | 0 | (m-1)(m-2)/2 | 0 | 0 |

Table 3: Comparison of elements, between different commercial available inverter with hybrid multilevel inverter

## VI. CONCLUSION

A 9-level symmetrical multilevel inverter topology has been discussed in this paper. The most main feature of the system is being convenient for expanding and higher the number of output levels with less number of bidirectional power electronics switches. This method results in the reduces of the number of switches, losses and cost of the multi level converter. Based on presented PWM switching scheme, the multilevel inverter generates approximately-sinusoidal output voltage and as a result, very has low harmonic profile.

This paper presented a topology for family of symmetrical cascade multilevel inverter. It has twelve bidirectional switches and a PWM scheme for determination of dc voltage source magnitudes too. This technique shows more flexibility to designers and can generate higher number of voltage levels without losing any level which worsens Total Harmonics Distortion characteristics. The possibility of increases or series connection of this basic cell. Matlab/Simulation results also illustrate the performance and effectiveness of the circuit for generates a high-quality and efficient output voltage waveform and harmonic profile of output voltage and current are low.

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