# Low-Voltage Boosted CMOS Drivers Ripple Carry Adder

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*Abstract*— In This paper, a modified high speed low voltage BCDL (Boosted CMOS differential logic) style to provide higher switching. This circuit is used in Ripple Carry Adders to improve switching speed by boosting the gate to source voltage to minimize the transistors along with timing critical signal path. The modified BCDL circuit to be shared by complementary outputs as a result also minimizes area. We carried out a comparison results against the existing logic design indicated that the propagation delay product of the modified logic style was improved by up to .35% compared with conventional logic style at supply voltage 1.8V. The test sets of logic gates and 32 bit adders where designed in TSMC 0.18µm CMOS process. The simulation result of 32bit Ripple Carry Adders using the modified logic style revealed that the addition time is reduced as compared with the existing conventional logic style.

***Key words:*** Low power, Threshold voltage, XOR gate

## I. INTRODUCTION

Bootstrapping is an efficient technique for speed enhancement and power reduction. One of the popular ways of reducing the power consumption of a CMOS digital circuit is to scaling down the supply voltage. Energy consumption of modern digital CMOS circuits has been traditionally dominated by switching energy having quadratic dependence on supply voltage scaling is an effective way to minimize the overall energy consumption of system-on a-chip. In the extreme case, circuits can be made to be operated in the sub-threshold region for maximum energy efficiency. However, the approach is limited to be only used in a low-end design, where speed is a secondary concern, because of severe speed degradation due to small switching current and high performance variability due to process, temperature, and threshold voltage variations. For medium and high end designs, where speed performance and energy efficiency are both important, that much aggressive voltage scaling is not acceptable, and instead, a near-threshold voltage design is more suitable for achieving relatively high energy efficiency without severe speed degradation.

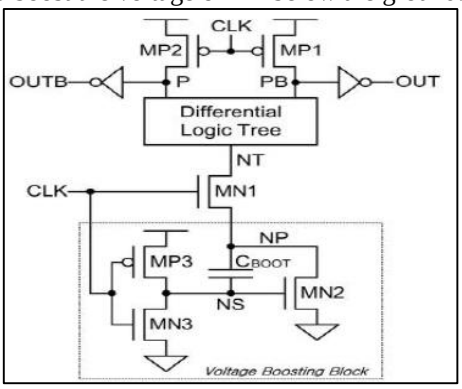
Existing physical layer design, the speed performance of circuits is not sufficient for high speed applications in differential cascade voltage switch (DCVS) logic .Domino CMOS logic is still severely degraded due to the reduced overdrive voltage of transistors. For fast logic operation at low supply voltage, CMOS bootstrapped dynamic logic (BDL) was proposed. However, the speed of this logic style was not so much improved since the latency of bulky bootstrapping circuit was superimposed on the overall latency of the circuit.

### *A. Outline Paper*

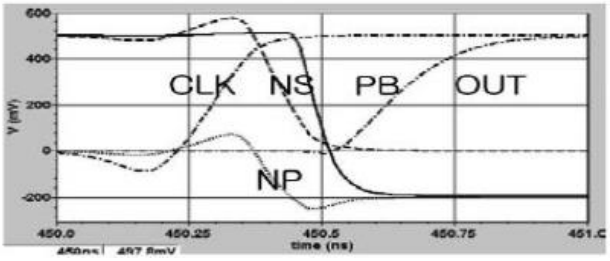
The rest of the paper is organized as follows: In section –II Describe the Boosted CMOS differential logic and previous BCDL circuit**, Section** III-Proposed BCDL Circuit, Section IV Simulation result.

## II. BOOSTED CMOS DIFFERENTIAL LOGIC (BCDL)

Fig.1 (a) shows a generic structure of the logic style, i.e., boosted CMOS differential logic (BCDL). It has two phases of operation, namely, a precharge phase and a boosted evaluation phase. The circuit is in the precharge phase when CLK is low. During this phase, the precharged differential logic block is separated from the voltage-boosting block since MN1 is fully off. Precharge nodes C and PB in the differential logic block are then precharged to the supply voltage by MP1 and MP2, letting outputs OUT and OUTB identically low. At the same time, transistors MP3 and MN2 in the voltage-boosting block turn on, allowing NS and NP to be high and low, respectively. Then, a voltage identical to the supply voltage is applied across CBOOT. When CLK changes to high, the circuit goes into th e boosted evaluation phase. The simulated waveforms of BCDL in this phase are shown in Fig. 2(b), where a supply voltage of 1.8 V is used. Since CLK goes high, MN1 turns on and connects the differential logic tree to the voltage-boosting block. At the same time, NS is pulled down toward the ground, allowing NP and NT to be boosted below the ground by capacitive coupling through CBOOT. It consists of a precharged differential logic block and a voltage boosting block. The voltage-boosting block, which is shown in the dotted box at the lower part of the circuit, is composed of transistors MN2, MN3, and MP3 and boosting capacitor CBOOT and is used to boost the voltage of NP below the ground.




(a)




(b)

Fig. 1: BCDL (a) Structure. (b) Simulated waveforms.

Jong-Woo Kim et al. [4] an 8 bit ripple carry chain was used in the BDCL adder to allow boosting operation of each carry chain stage. Fig.2 shows the conventional structure of 8 bit ripple carry chain used in the BDCL adders.

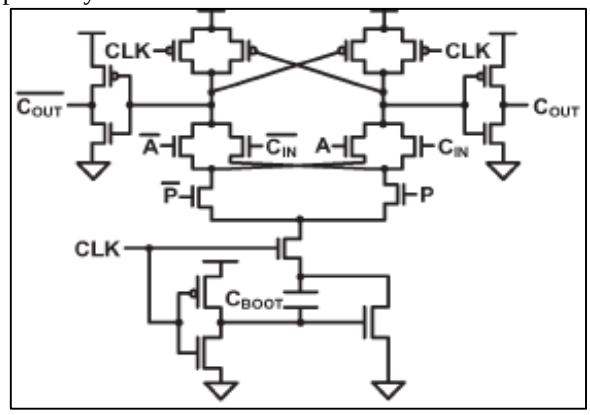



Fig. 2: Conventional Structure of an 8-bit Ripple Carry

## III. PROPOSED RIPPLE CARRY ADDER

Fig. 3 shows the proposed structure of the Boosted CMOS ripple carry adder. The advantage of the proposed circuit is not depending on the A input. It's depend on clock plus. The A and Ā input are replaced to the CLK and $\overline{CLK}$ pulse. Fig.4 shows the waveform of proposed ripple carry adder .

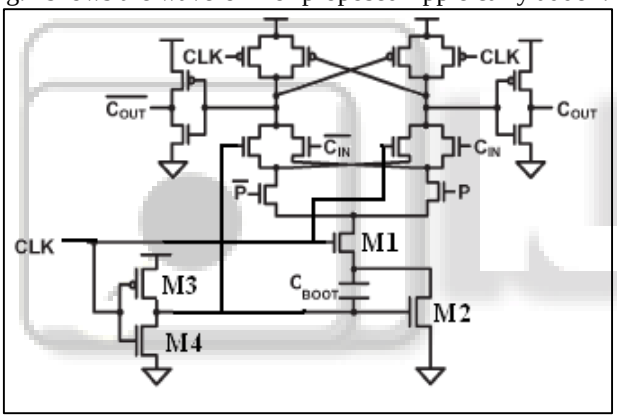



Fig. 3: Proposed Structure of an 8-bit Ripple Carry chain in BCDL

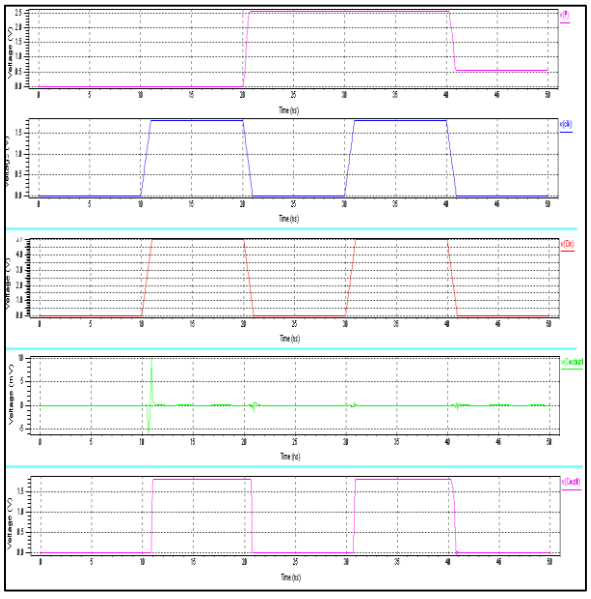


Fig. 4: Proposed 8-Bit Ripple Carry Adder Waveform.

To demonstrate practical applicability of the proposed logic style, a set of 32-bit adders were designed. The 32-bit adder consisting of eight 8-bit adder subsections adopts the carry selection scheme for high-speed carry propagation. In BCDL Adder an 8-bit ripple carry chain was used to allow boosting operation at each carry chain stage for high-speed carry propagation. Fig. 7 shows the structure of the 8-bit ripple carry chain used in the 32-bit BCDL adder.

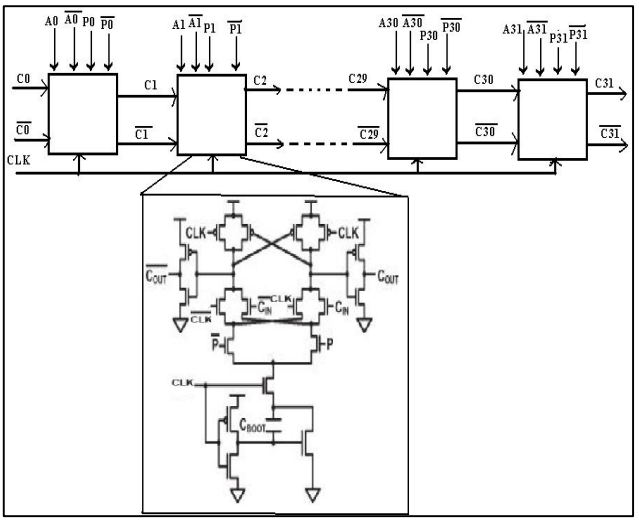



Fig. 7: Structure of an 1-bit ripple carry chain in a 32-bit BCDL adder

### *A. Fir Filter*

Using this BCDL Logic FIR Filter is designed. it consist of 32-Bit Carry Select Adder and 8x8 Array Multiplier.

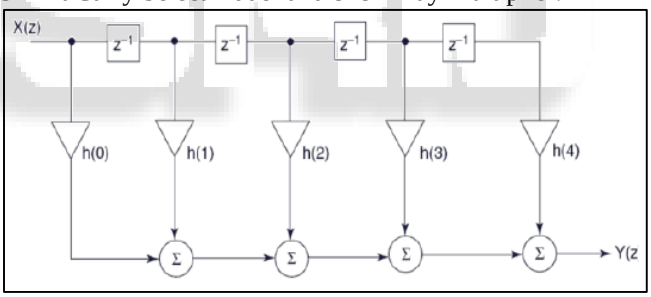



Fig. 8: BCDL Logic FIR Filter

In the place of h(0),h(1),h(2)….h(4) 4x4 Array Multiplier is implemented.

### *B. 4X4 Array Multiplier*

The array multiplier desire to speed up the rate at which the output is generated resulted in the development of this category of multiplier. In a serial-parallel multiplier discussed above, it takes one clock cycle to process one bit of the data input at any given time. Therefore, when working on an N-bit input it would take at least N clock cycles to generate the final output.

In an array multiplier the result is obtained as soon as inputs are presented to the multiplier. This is mainly because of the use of AND array structure to compute the partial product terms. Once the partial product terms are generated the only delay in generating the output is contributed by the adders which sum the partial product terms column wise to generate the result. The figure below represents a parallel array multiplier with N=4 bit inputs.

The modified technique is general and can be used in all domino logic circuit designs. Higher order multipliers like 16x16, 32x32 may also be implemented using 4x4 bit multiplier and hence a modular design is presented by constructing an 8x8 multiplier using multiple 4x4 multipliers.

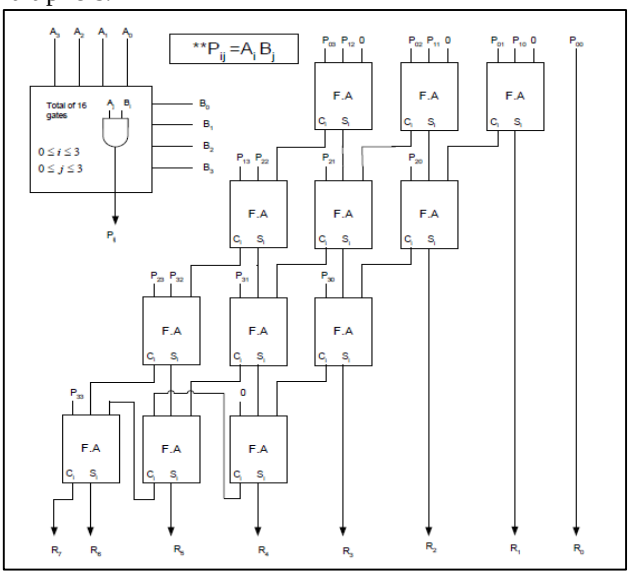



Fig. 9: 4* 4 Array Multiplier

## IV. Simulation Results

To assess the performance of the proposed circuit technique, various multi-input logic gates are designed using the conventional and proposed logic styles in a TSMC 0.18-$\mu$m CMOS process. The boosting capacitor $C_{BOOT}$ was implemented using the gate-oxide capacitance of a pMOS transistor. Transistor widths in each logic gate and the amount of boosting capacitance were individually optimized at each supply voltage for each logic style to provide a minimum propagation delay product (PDP).

The table I summarizes the simulated performance of ripple carry adder designed with the conventional and proposed logic styles. The simulation was executed at 100-MHz frequency with a supply of 1.8V. The fig.4 shows the graph of delay, power consumption and PDP.

| Ripple Carry Adder | Total delay(ns) | Power consumption(µm) | PDP |
|---|---|---|---|
| 22T (Prop.) | 19.54 | 16 | 313 |
| 24T | 19.61 | 16 | 314 |

Table. 1: bit ripple carry adder

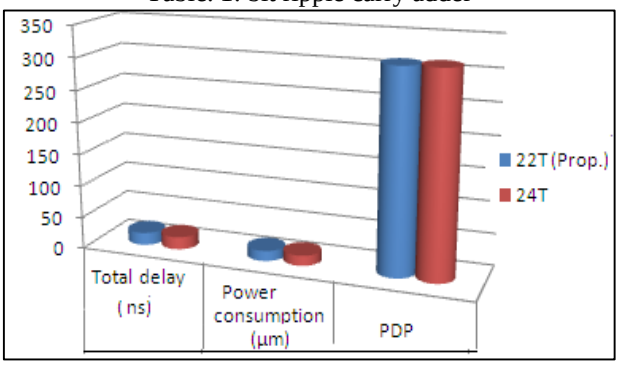



Fig. 4: Delay, Power consumption & PDP Chart of 1 bit ripple carry adder

The measured propagation delay and switching energy of the BCDL adder depending on supply voltage are summarized in Table 2 of 32 bit ripple carry adder. The simulation was executed at 100-MHz frequency with a supply of 1.8V. The fig.5 shows the graph of delay, power consumption and PDP.

| 32 bit Ripple Carry Adder | Total delay( ns) | Power consumption(µm) | PDP |
|---|---|---|---|
| 704T (Prop.) | 19.57 | 10 | 195 |
| 768T | 19.61 | 10 | 196 |

Table 2: 32 bit ripple carry adder

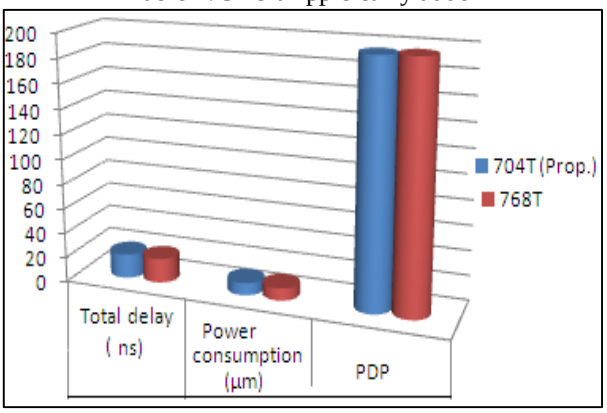



Fig. 5: Propagation Delay, Power consumption & PDP Chart of 32 bit ripple carry adder

## V. Conclusion

In this paper brief, a high speed Low voltage BCDL has been described which is applicable in Ripple Carry Adders. This circuit is depends on the clock pulse. The modified BCDL circuit used in Ripple Carry Adders to enhance the higher switching speed by boosting the gate-source voltage of transistors and also minimize area. The modified logic circuit as compared to the existing circuit the propagation delay is improved. All the comparison results in a TSMC 0.18µm CMOS process. All the simulation results for 32bit Ripple Carry Adders using the modified logic style revealed that the addition time is reduced as compared with the existing conventional circuits.

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