Design and Implementation of PID Controller using HDL on FPGA: A Review

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Abstract— This paper concentrates on the work done on the PID control system using field programmable gate array (FPGA) technology. FPGA based realization offers high speed, complex functionality, consume less power, and provides parallel processing. Proportional-integral-derivative (PID) controller is a vastly used control algorithm for many real-time control applications. The different works which have already been done are summarised here like gain margin methods, DC motor using Pulse Width Modulation, Intelligent PID controller based on Very large scale integrated circuits (VLSI). In this paper, we focused our works designing PID controller by Field Programmable Gate Arrays (FPGAs) with some parameter change so that the cost will be minimized and accuracy will be maximized. This survey paper covers the study on such methods that compensates these terms.

Key words: PID Control, HDL, FPGA, Control System

I. INTRODUCTION

PID controllers are the most popular controller system used in industries, Proportional-Integral-Derivative (PID) controllers are universal control structure and have widely used in Automation systems, and they are usually implemented either in hardware using analog components or in software using Computer-based systems. Proportional Integral Derivative (PID) based scheme is widely preferred in industries because of their simple structure and ease of realization. Project is to design a PID controller and implement it on FPGA using hardware description language. PID controller along with PWM module is used for speed control of DC motor and current – voltage control of DC – DC converter. Proportional-Integral-Derivative (PID) controllers are still dominating in the motion control systems in the industry due to the well acquaintance of the operating personnel with PID controllers.

II. PID CONTROLLER

The PID algorithm consists of three modes proportional, integral and derivative mode.

PID algorithm consists of three basic coefficients:

- Proportional: For Proportional $p(t) = Kp*e(t)$
- Integral: For integral $i(t) = Ki*\int e(t)dt$
- Derivative: For derivative $d(t) = Kd* de(t)/dt$

The PID controller follows the classical structure, contains two saturation blocks, one for the integral part and the other for the overall sum. The controller has a pipeline structure of three stages, in other words, it needs three clock cycles to perform all the operations. In order to improve the area and speed, hardware multipliers have been used. Building PID controllers on Field Programmable Gate Arrays (FPGAs) which improve speed, power and cost effectiveness.

G.SHYAMALA [5] has presented a novel way to implement digital controllers with a successful implementation of a digital PID controller. The design shows significant improvements over the present way of implementing digital controllers in Microcontroller Units in terms of latency, response, flexibility, and robustness. In this paper the PWM module is used, PWM generator and the encoder interfacing module has been implemented in the FPGA. The entire system has been simulated using the Xilinx ISE.

A. FPGA Development Board

FPGA, a PLD is a semicustom component, which includes configurable logic blocks, input-output blocks and interconnects. It has some important characteristics; highly integrated, fast computer speed, could be parallel programmed and online programmed.

III. LITERATURE REVIEW

The main aim of this paper [1] is to design PID control PWM module using field programmable gate array (FPGA) technology. FPGA based realization offers high speed, complex functionality, consume less power, and provides parallel processing. In this paper, we have implemented PID control PWM module on programmable logic design software Quartus II and verified on DE0 Nano Board (Cyclone IV FPGA family of company Altera). Signal Tap II analyzer and RTL viewer are used for analyzing and debugging the design. For Proper timing constraint and clock arrangement, Time Quest analyzer is used. The simulation and hardware results shows that implementation with FPGA has some advantages such as flexible design, high reliability and high speed. Proportional-Integral-Derivative (PID) controllers [2] are universal control structure and have widely used in Automation systems, they are usually implemented either in hardware using analog components or in software using Computer-based systems. In this paper, we focused our works designing on building a multi-channel PID controller by Field Programmable Gate Arrays (FPGAs). To overcome the hardware complexity by the use of more processors for multi-channel, using single PID controller for multi-channel .Multi channel can be implemented by the use of FPGA. When the error is more it can differentiate and produce the constant output, when signal is low when compared to reference signal it can integrate it. FPGA can offer parallel processing, more speed.

The main objective of this paper [3] is to present the steps of how to program a PID controller in a FPGA, and in that way to control a DC motor using Pulse Width Modulation. Also we want to give some ideas to people interested in program embedded controllers in hardware. During the project use some tools to help us to visualize the behavior of the controller on the computer screen through rs232 communication and LabView chart to plot, and LCD display for visualize the Set Point, gains and the current value PID (Proportional – Integral - Derivative) controllers are the

most widely used closed loop controllers due to their simplicity, robustness, effectiveness and applicability for much kind of systems [4]. With the rapid development of technology, implementation of PID controller has gone several steps from

Using analog components in hardware to using some software based program to execute PID instructions digitally in some processor-based systems. And also, these developments have brought an alternative solution to implement PID instructions in Programmable Logic Devices (PLD). Field Programmable Logic Array (FPGA) is the most advanced members of PLDs. This paper [4] presents the digital PID algorithm on FPGA. The controller algorithm is developed using VHDL and implemented using Altera DE0 Nano Board. As the controlled system, five axis robot arm is selected, which have five dc motor and four potentiometer to determine the positions of motors. The results show that digital PID controller and also multi-feedback control systems can be implemented successively using FPGA devices.

This paper presents [5] a novel technique for implementation of an efficient FPGA based digital Proportional-Integral-Derivative (PID) controller for the motion control of a permanent magnet DC motor. The implementation technique circumnavigates the problem of interfacing analog and digital systems in real-time. The controller is used in a speed control loop. This paper [6] explains a method for the design of Intelligent PID controller based on Very large scale integrated circuits (VLSI). In PID controller parameters are tuned with particle swarm optimization (PSO) algorithm. The error is identified and the PSO algorithm controls the system with many iteration of different parameters**.**

This paper [7] presents the implementation of a proportional-integral-Derivative (PID) controller for motion control of a DC motor based on FPGA. This implementation technique used to avoid the problems which create during analog and digital interfacing system in real-time. The controller used in speed controller loop. The hardware implementation has been done on a Xilinx Spartan 3 FPGA chip and generates the PWM signal as an input of motor driver for controlling. The out of optically encoded data is decoded and give it to PID control loop. Proposed implementation is present through the VHDL algorithm.

IV. Conclusions

This paper presents a brief review of recent researches and their techniques for optimizing the output of PID control system. Though there are many control systems are available, PID is the best and mostly used in control system. By using FPGAs, this paper implemented PID control system digitally. FPGAs are more useful than any other digital system. This proposed architecture can be useful for real time control system applications. The diversity of researches done by various researchers have summarized and studied in this paper.

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References

[1] Implementation of a PID control PWM module on altera DE0 kit using FPGA by Ruchi Jain and M.V. Aware, Conference Paper January 2016.
[2] International Journal of Soft Computing and Engineering (IJSCE) ISSN: 2231-2307, Volume-3, Issue-1, March 2013 Design & Implementation of PID Controller Based On FPGA with PWM Modulator by Rajesh Nema, Rajeev Thakur, Ruchi Gupta.
[3] Advanced Digital Technologies – Universidad Pontificia Bolivariana – October 2011 Implementation Of a PID Controller Embedded In a FPGA For Positioning A DC Motor.
[4] Multiple Closed Loop System Control with Digital PID Controller Using FPGA by Şirin AKKAYA and Onur Akbatı and Haluk Görgün in 978-1-4799-6773-5/14/$31.00 ©2014 IEEE.
[5] Digital PID Controller Implementation for Speed Control Applications Using FPGA by G. Shyamalal, M. Gurunadha Babu2, R. Muni Praveena Rela3.
[6] Design of Intelligent PID Controller Based On Particle Swarm Optimization In FPGA International Journal of Power Control Signal and Computation (IJPCSC) by S.Karthikeyan Dr. P. Rameshbabu, Dr.B.Justus Robi
[7] Sandeepa Prabhu1, Praveen Konda K2 1ECE Department, Sahyadri College Of Engineering and Management, India IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 6, Issue 3, Ver. II (May. -Jun. 2016), PP 116-121 e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
[8] T. Morkel, J.H.P. Eloff, M.S. Olivier, 'An Overview Of Image Steganography', Information and Computer Security Architecture (ICSA) Research Group, Department of Computer Science, University of Pretoria, 0002, Pretoria, South Africa.
[9] Michael Eung- Min Lee "Mathematical Models of the Carding Process" St. John's College,University of Oxford.
[10] Dr. Sarina Binti Shafie "COIL WINDING MACHINE" Faculty of Manufacturing Engineering, Universiti Malaysia Pahang.

