Low-Power and Area-Efficient Shift Register Using Pulsed Latches

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Abstract— The Shift Register is another type of sequential logic circuit that can be used for the storage or the transfer of data in the form of binary numbers. A power-efficient shift register utilizing a new flip-flop with a pulse-triggered structure is presented in this paper. The proposed flip-flop has features of high performance and low power. The key idea was to design in various performance aspects provide a signal feed through from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance. The design was intelligently achieved by employing a simple pass transistor. The proposed design successfully solves the long discharging path problem in conventional explicit type pulse-triggered FF (P-FF) designs and achieves better speed and power performance. Based on post-layout simulation results using CMOS 90-nm technology. The best power-delay-product performance in seven FF designs under comparison. Its maximum power saving against rival designs is up to 38.4%.Compared with the conventional transmission gate-based FF design.

Key words: Area-Efficient, Flip-Flop, Pulsed Clock, Pulsed Latch, Shift Register

I. INTRODUCTION

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs now a-days often adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and first in-first out. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 50% of the total system power. FFs thus contribute a significant portion of the chip area and power consumption to the overall system design [2], [3]. Depending on the method of pulse generation, P- FF designs can be classified as implicit or explicit [7]. In an implicit-type P-FF, the pulse generator is a built- in logic of the latch design, and no explicit pulse signals are generated. In an explicit-type P-FF, the designs of pulse generator and latch are separate. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. This is because the former merely controls the discharging path while the latter needs to physically generate a pulse train. Implicit-type designs, however, face a lengthened discharging path in latch design, which leads to inferior timing characteristics. The situation deteriorates further when low-power techniques such as conditional capture, conditional recharge, conditional discharge, or conditional data mapping are applied [4]–[6]. As a consequence, the transistors of pulse generation logic are often enlarged to assure that the generated pulses are sufficiently wide to trigger the data capturing of the latch. Explicit-type P-FF designs face a similar pulse width control issue,

II. SHIFT REGISTERS

A shift register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters, communication receivers and image processing ICs Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register A 16- megapixel CMOS image sensor uses a 45K-bit shift register. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches.

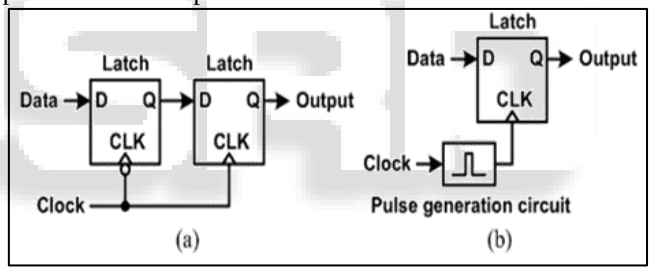


Fig. 1: (a) Master-slave flip-flop. (b) Pulsed latch.

This paper proposes a low power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. Shift registers can have both parallel and serial inputs and outputs. These are often configured as 'serial-in, parallel-out' (SIPO) or as 'parallel-in, serial-out' (PISO). There are also types that have both serial and parallel input and types with serial and parallel output. There are also 'bidirectional' shift registers which allow shifting in both directions: L→R or R→L. The serial input and last output of a shift register can also be connected to create a 'circular shift register' previous work often measured energy consumption using a limited set of data patterns with the clock switching every cycle. But real designs have a wide variation in clock and data activity across different TE instances. For example, low power microprocessors make extensive use of clock gating resulting in many TEs whose energy consumption is dominated by input data transitions rather than clock transitions. Other TEs, in contrast, have negligible data input activity but are clocked

every cycle. Shift registers, like counters, are a form of sequential logic. Sequential logic, unlike combinational logic is not only affected by the present inputs, but also, by the prior history. In other words, sequential logic remembers past events. Pulsed latch structures employ an edge-triggered pulse generator to provide a short transparency window. Compared to master–slave flip-flops, pulsed latches have the advantages of requiring only one latch stage per clock cycle and of allowing time borrowing across cycle boundaries. The major disadvantages of pulsed latch structures are the increased susceptibility to timing hazards and the energy dissipation of the local clock pulse generators.

III. EXISTING SYSTEM

Pulse-triggered Flip Flop (P-FF) has been considered a popular alternative to the conventional master–slave-based FF in the applications of high-speed operations. Besides the speed advantage, its circuit simplicity is also beneficial to lowering the power consumption of the clock tree system. A P-FF consists of a pulse generator for generating strobe signals and a latch for data storage. Since triggering pulses generated on the transition edges of the clock signal are very narrow in pulse width, the latch acts like an edge-triggered FF. The circuit complexity of a P-FF is simplified since only one latch, as opposed to two used in conventional master–slave configuration, is needed. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. P-FFs are thus less sensitive to clock jitter. Despite these advantages, pulse generation circuitry requires delicate pulse width control in the face of process variation and the configuration of pulse clock distribution network.

Depending on the method of pulse generation. Pulse-triggered flip-flops can be classified into two types, implicit and explicit, and this classification is due to the pulse generators they use. In implicit-pulse triggered flip-flops (ip-FF), the pulse is generated inside the flip-flop, for example, hybrid latch flip-flip (HLFF), semi-dynamic flip-flop (SDFF), and implicit-pulsed data-close-to-output flip-flop (ip-DCO). Whereas, in explicit-pulse triggered flip-flops (ep-FF), the pulse is generated externally, for example, ex-plicit-pulsed data-close-to-output flip-flop (ep-DCO).

A. Pulse Triggered Flip Flop (PTFF)

In Implicit-type P-FF designs, which are used as the reference design in later performance comparisons, are first reviewed. A state-of-the-art P-FF design is given in Fig. It contains an AND logic-based pulse generator. Inverters I5 and I6 are used to latch data and Inverters I7 and I8 are used to hold the internal node X. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters I1-I3.

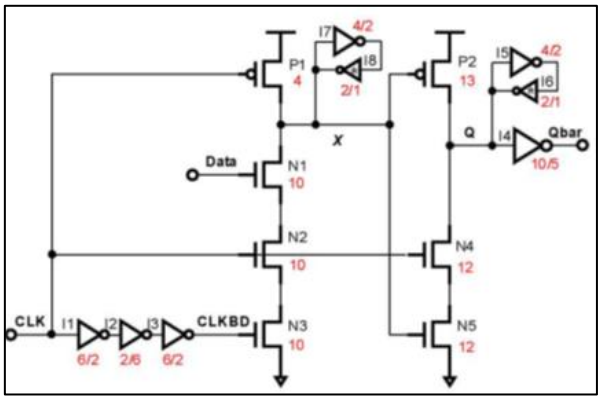


Fig. 3.1: Pulse-triggered Flip Flop

Two practical problems exist in this design. First, during the rising edge, nMOS transistors N2 and N3 are turned on. If data remains high, node X will be discharged on every rising edge of the clock. This leads to a large switching power. The other problem is that node X controls two larger MOS transistors (P2 and N5). The large capacitive load to node X causes speed and power performance degradation.

B. Hybrid Latch Flip-Flop (HLFF)

Improved P-FF design, named MHLLF, by employing a static latch structure presented. Node X is no longer pre charged periodically by the clock signal. A weak pull-up transistor P1 controlled by the FF output signal Q is used to maintain the node X level at high when Q is zero. This design eliminates the unnecessary discharging problem at node X. However, it encounters a longer Data-to-Q (D-to-Q) delay during "0" to "1" transitions because node X is not pre-discharged. Larger transistors N3 and N4 are required to enhance the discharging capability.

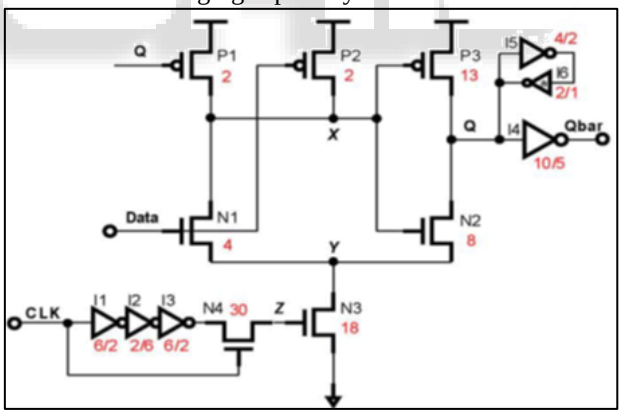


Fig. 3.2: Hybrid Latch Flip Flop

C. SCCER Design

Low power P-FF design named SCCER using a conditional discharged technique. In this design, the keeper logic (back-to-back inverters I7 and I8 in Fig. 1(a)) is replaced by a weak pull up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node X. The discharge path contains nMOS transistors N2 and N1 connected in series. In order to eliminate superfluous switching at node X, an extra nMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high. The worst case timing of this design occurs when input data is "1" and node X is discharged through four transistors in series, i.e., N1 through N4, while combating with the pull up

transistor P1. A powerful pull-down circuitry is thus needed to ensure node X can be properly discharged. This implies wider N1 and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

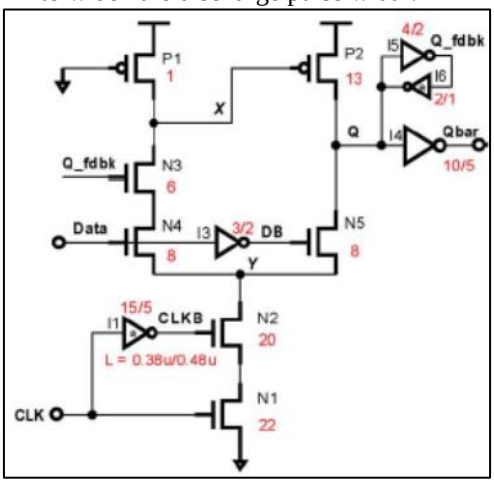


Fig. 3.3 SCCER Flip Flop

IV. PROPOSED SYSTEM

The proposed design adopts two measures to overcome the problems associated with existing P-FF designs. The first one is reducing the number of nMOS transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when input data is "1." Refer to Fig. 2, the upper part latch design is similar to the one employed in SCCER design [12]. As opposed to the transistor stacking design in Fig. 1(a) and (c), transistor N2 is removed from the discharging path. Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate [13], [14] to control the discharge of transistor N1. Since the two inputs to the AND logic are mostly complementary (except during the transition edges of the clock), the output node _ is kept at zero most of the time. When both input signals equal to "0" (during the falling edges of the clock), temporary floating at node _ is basically harmless. At the rising edges of the clock, both transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node _, which then turns on transistor N1by a time span defined by the delay inverter I1. The switching power at node _ can be reduced due to a diminished voltage swing. Unlike the MHLLF design [11], where the discharge control signal is driven by a single transistor, parallel conduction of two nMOS transistors (N2 and N3) speeds up the operations of pulse generation. With this design measure, the number of stacked transistors along the discharging path is reduced and the sizes of transistors N1-N5 can be reduced also.

In this design, the longest discharging path is formed when input data is "1" while the Q bar output is "1." To enhance the discharging under this condition, transistor P3 is added. Transistor P3 is normally turned off because node □ is pulled high most of the time. It steps in when node □ is discharged to □□□_□ below the □__. This provides additional boost to node _ (from □___□□_ to □__). The generated pulse is taller, which enhances the pull-down strength of transistor N1. After the rising edge of the clock, the delay inverter I1 drives node _ back to zero through transistor N3 to shut down the discharging path. The voltage level of Node□ rises and turns off transistor P3 eventually. With the intervention of P3, the width of the generated discharging pulse is stretched out. This means to create a pulse with sufficient width for correct data capturing, a bulky delay inverter design, which constitutes most of the power consumption in pulse generation logic, is no longer needed. It should be noted that this conditional pulse enhancement technique takes effects only when the FF output _ is subject to a data change from 0 to 1. The leads to a better power performance than those schemes using an indiscriminate pulse width enhancement approach. Another benefit of this conditional pulse enhancement scheme is the reduction in leakage power due to shrunken transistors in the critical discharging path and in the delay inverter.

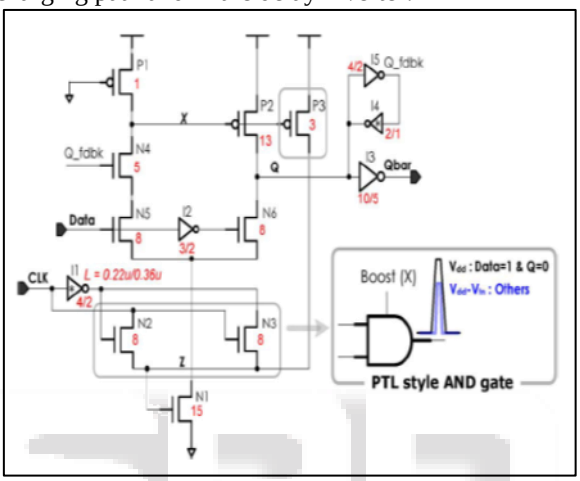
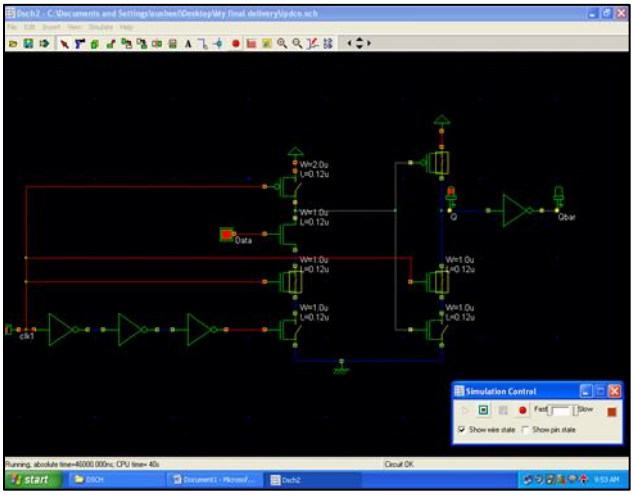


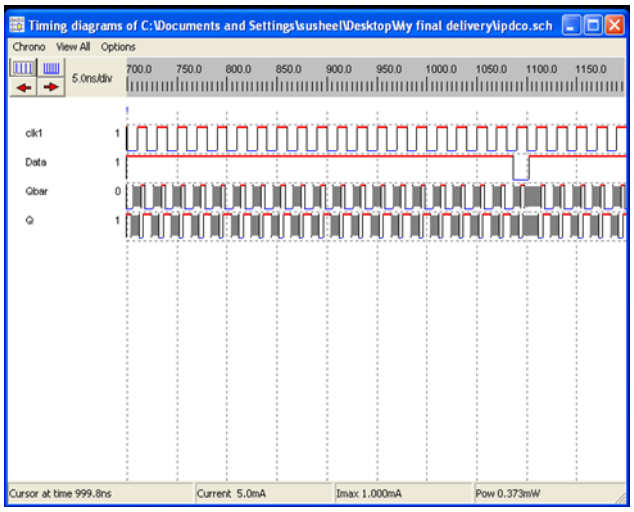
Fig. 4.1: Schematic of the proposed P-FF design with pulse Control Scheme

V. SIMULATION RESULTS

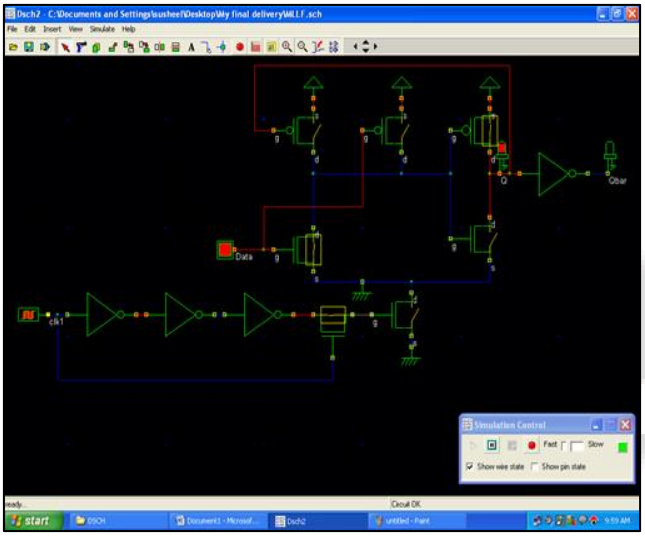
A. IP-DOC Schematic Design



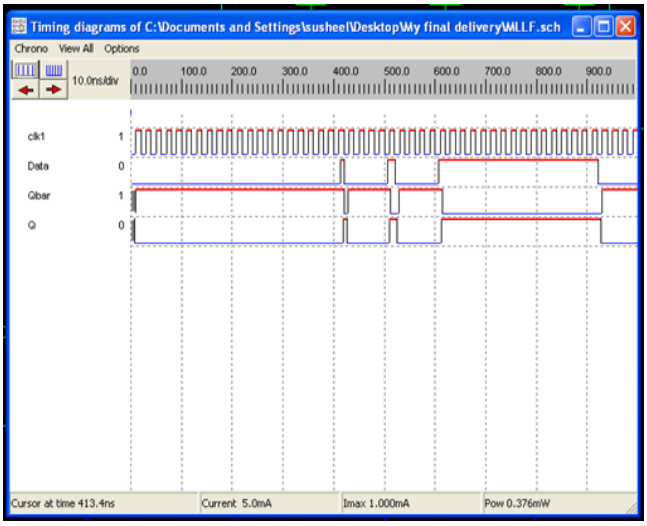
B. IP-DOC Output Waveforms



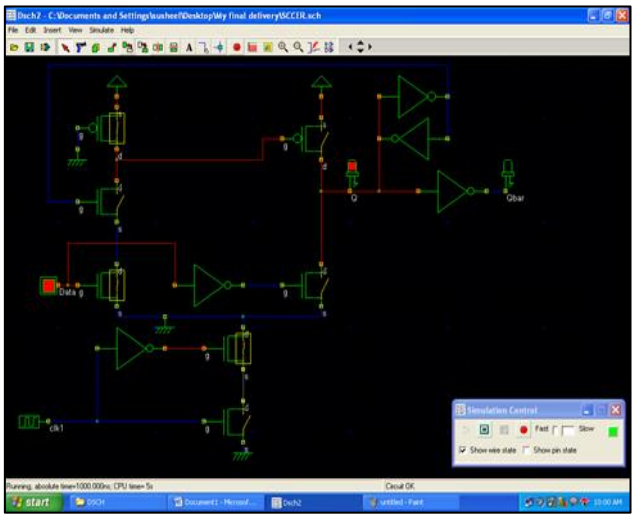
C. MLLFF Schematic Design



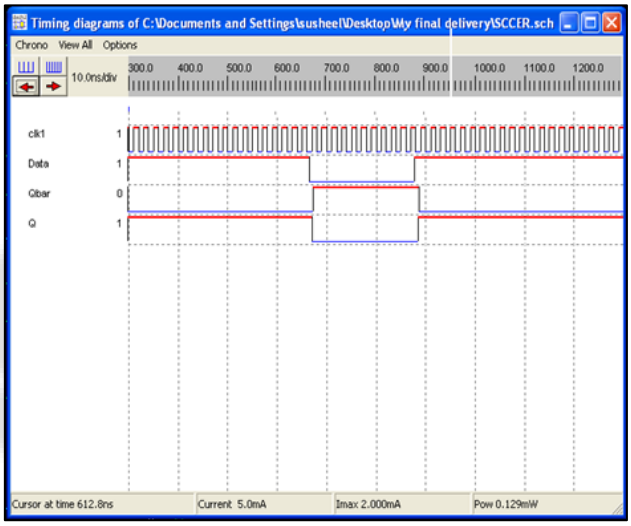
D. MLLFF Output Wave Form



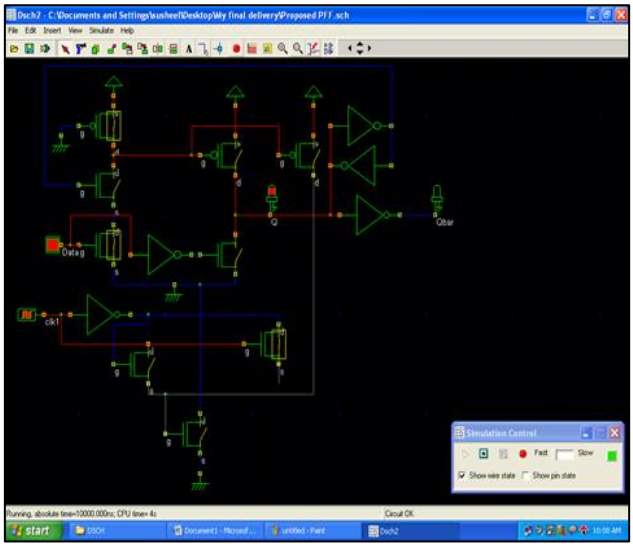
E. SCCER Schematic Design



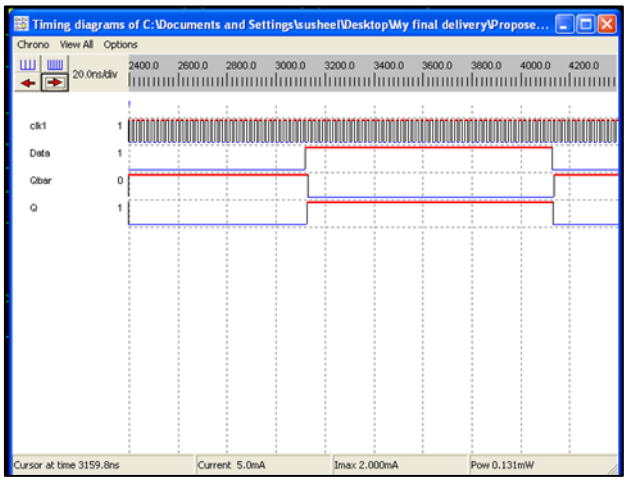
F. SCCER Output Wave Form.

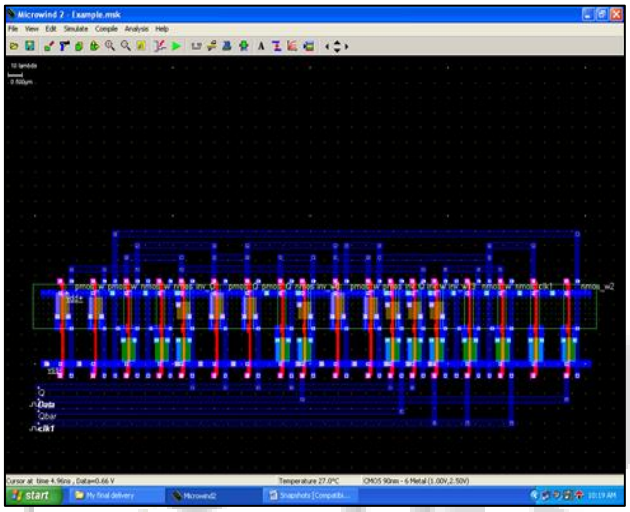


G. Proposed PFF Schematic

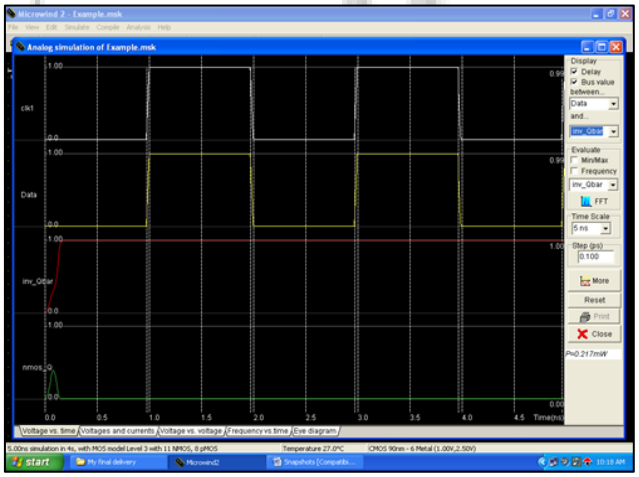


H. Proposed PFF Output





I. Proposed PFF Output Wave Form



VI. CONCLUSION

This paper proposed P-FF which is used to design low-power and area-efficient shift register for reduction of area and power consumption by replacing flip-flops with P-FF. The various Flip flop design like, ip-DCO, MHLLF and SCCER are discussed. These were been also designed in Wicrowind tool and those result waveforms are also discussed. With these all results SCCER performed better than ip-DCO and MHLLF designs.

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