Reduction of Harmonics by using Single Stage Boosting Inverter with Trap-CL Filter for PV Applications

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Abstract— The single stage boosting inverter with trap-CL filter for alternative energy generation is used to reduce the Total Harmonic Distortion (THD). It has a simpler topology and a lower component count. One cycle control was employed to generate AC voltage output. The Total Harmonic Distortion is considering while designing an output filter. In PV module, the size and the weight also have to be taken into consideration. The proposed output filter consists mainly of conventional CL-filter with a trap filter. This paper is used to achieve voltage boosting and eliminating the harmonics at switching frequency, good quality of AC output waveform. This project is implemented for 1 kW (voltage=60v) solar panel by using MATLAB Software.

Key words: Single Stage Boosting Inverter, One Cycle Control (OCC), Tapped Inductor (TI), Trap-CL Filter, Harmonics Reduction, Photovoltaic Panel

I. INTRODUCTION

Micro inverter topologies for photovoltaic (PV) power generation are classified into three major groups: the single-stage, the two stage, and the multi-stage types. The multistage micro inverters are usually comprised of a step up dc–dc converter front stage, under maximum power point tracking (MPPT) control, an intermediate high-frequency dc–dc converter stage, used to attain a rectified-sine waveform, and a low frequency unfolding stage to interconnect to the grid [1]. However, the multistage power train and the associated high component count result in a costly product. The two-stage micro inverter can be designed cascading a MPPT-controlled Step up dc–dc converter and a grid-tied high-frequency inverter, whereas the single-stage topology has to perform the voltage step up, the MPP tracking, and the dc–ac inversion functions all in one stage [2].

In order to convert and connect the solar energy to the grid, the low voltage of the PV panel first has to be stepped up significantly to match the utility level. Another concern, typical to single-phase dc–ac power systems, is ac–dc power decoupling problem [3]-[5]. A traditional solution is application of a decoupling capacitor on the dc-link between the input and output stages. The value of the decoupling capacitor depends on the rated power P_{dc}, the line frequency f, and the average voltage across the capacitor V_{dc}, and the allowed peak-to-peak ripple Δv

$$C_{dc} = \frac{P_{dc}}{2\pi f \Delta v V_{dc}}$$

The two-stage or the multistage micro inverters can have their decoupling capacitor on the high voltage dc link, and, according to, attain lower value of the decoupling capacitor. However, some single stage micro inverters may require placing the decoupling capacitor at the PV module terminals. The low panel voltage, V_{dc}, and the desired low ripple, Δv, see, result in a substantial decoupling capacitor value and size In field conditions, large electrolytic capacitors have short life and impair system's reliability. Therefore, the power decoupling problem becomes one of major concerns in micro inverter design. Application of small non electrolytic capacitors is strongly desired. To minimize the decoupling capacitor, additional power decoupling circuits were suggested in literature. A fly back-type single-stage topology with an additional power decoupling circuit proposed in reported a decoupling capacitor of only 40μF. However, the efficiency was only 70%. An improved topology employing leakage energy recycling demonstrated 86% peak efficiency. Some other fly back-based topologies also make use of an additional power decoupling circuit.

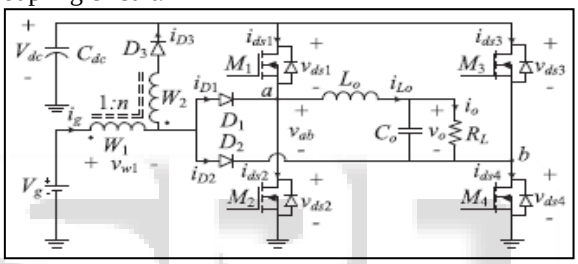

Fig. 1: SSBI Topology

In this paper, a single-stage boosting inverter (SSBI) is proposed for alternative energy/solar power generation. SSBI can attain higher dc gain and, thus, operate off low dc input voltage of a single PV panel. By its concept of operation SSBI shares the switches of the power train in a manner that allows merging the dc–dc step-up converter stage and the grid-tied dc–ac inverter stage. Hence, SSBI is realized in a single stage [6]. The power decoupling is performed at high voltage; thus, low value of dc-link decoupling capacitor is required. The SSBI easily lends itself to application of one cycle control (OCC), which helps attaining high-quality ac output regardless of low frequency ripple across the dc link [7]-[9]. However, any other control method can be applied.

II. DESCRIPTION OF THE PROPOSED TOPOLOGY

SSBI is comprised of semiconductor switches $M_{1\ldots4}$, arranged in a full-bridge configuration; steering diodes D_1, D_2; dc-link diode D_3, the tapped inductor (TI) W_1:W_2; the decoupling capacitorC_{dc}; and the output filter $L_o - C_o$. The load is represented by the resistorR_l.

The proposed SSBI is fed by a dc voltage source, Vg, considered to be derived of a single PV panel, and generates utility level ac output voltage Vo. Here, the input current is designated as i_o , the output current is i_o and its average component is Io[10]. the proposed SSBI topology has the advantages of a larger voltage step up which can be achieved adjusting the TI turns ratio, and smaller decoupling capacitor, which is placed on high voltage dc bus [11]-[14].

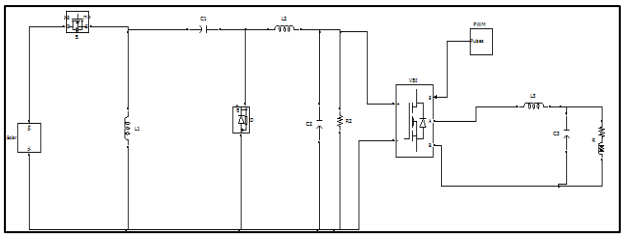

Fig. 2: Circuit Diagram of Two stage inverter (Existing)

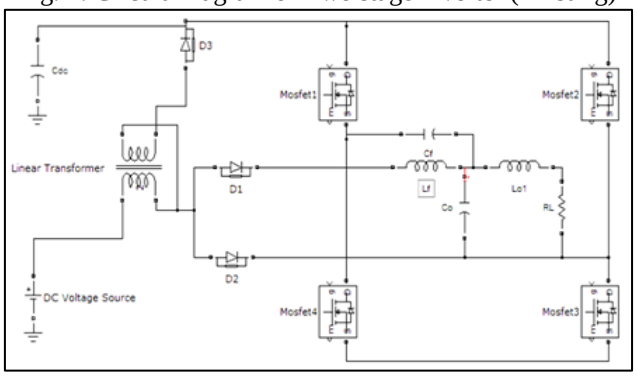

Fig. 3: Circuit Diagram of Single stage Boosting inverter (Proposed)

The switching cycle starts with State A, which lasts for a duration of t_a. Here, the switches M_1 and M_4 are ON, whereas switches M_2 and M_3 are OFF, D_2 conducts and D_1, D_3 are cut-off. During this state, the TI primary magnetizing inductance L_m is charged from the input voltage source V_g, while the dc voltage V_{dc} is applied to the input terminals of the output filter so the filter inductance L_o is charged feeding also the filter capacitor C_o and the load R_L.

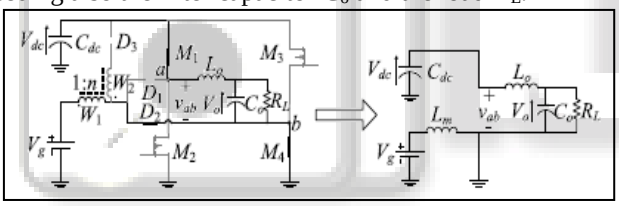

Fig. 4: State A of SSBI

State B commences, as the switch M_1 is turned off and M_2 is turned on, whereas M_4 keeps conducting. State B lasts for a duration of t_b. Here, both D_1 and D_2 conduct while D_3 is cut-off. As a result, the TI magnetizing inductance Lm continues charging from the input voltage source V_g, whereas the input terminals of the output filter are shorted so the filter inductance Lo is discharged to the output capacitor C_o and the load R_l.

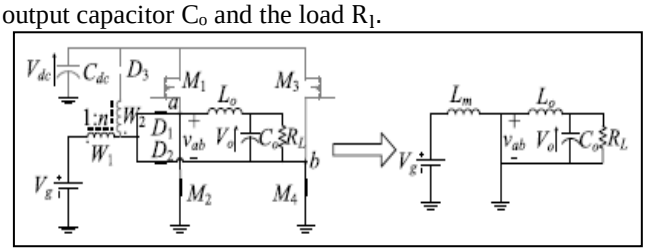

Fig. 5: State B of SSBI

State C begins as the switches M_1, M_3 are turned on and M_2,M_4 are turned off. State C lasts for duration of t_c , and completes the switching cycle. Here, both D_1 , D_2 are cut-off and D_3 conducts; the TI magnetizing inductance Lm is discharged via both windings and D_3 into the dc-link capacitor C_{dc}, while the input terminals of the output filter are shorted and the filter inductance L_o feeds the output capacitor C_o and the load R_l.

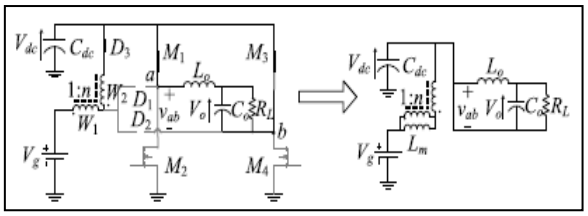

Fig. 6: State B SSBI

In order to generate output voltage of negative polarity, complementary switching states A`, B`, and C` are created by the controller [15]. Switching states of semiconductor devices throughout the switching cycle. To create the desired switching states, proper switching signals for the H-bridge switches should be generated of the given buck and boost switching functions and the output polarity signal $S_{bk}(D_{bk})$, $S_{bst}(D_{bst})$, P, respectively. Here, the driving signals of the switches M1 . . . M_4 are designated as S_1 . . .S_4, respectively. The required Boolean functions can be derived from Table.

$$S_1 = \overline{P \cdot S_{bk}} \cdot S_{bst}$$
$$S_2 = \overline{P \cdot S_{bk}} \cdot S_{bst}$$
$$S_3 = \overline{\overline{P} \cdot S_{bk}} \cdot S_{bst}$$
$$S_4 = \overline{\overline{P} \cdot S_{bk}} \cdot S_{bst}.$$

Note that since the switching cycle of SSBI is comprised of three states, there are 3! Possible permutations or state sequences [16]. In other words, the order of appearance of the states is not unique and other possibilities exist, i.e. A–C–B, C–B–A, etc. An ideal SSBI can generate same dc–dc conversion ratio under any of these switching regimes.

However, some state sequences may require switches to be activated twice per switching cycle, which is undesirable in practice due to increased switching loss and/or extremely narrow on time. Proper synchronization of the gating signals also requires attention [17]-[19].

The advantage of the implemented A–B–C state sequence is that each switch is turned on and off only once in a switching cycle, which helps reducing the switching losses.

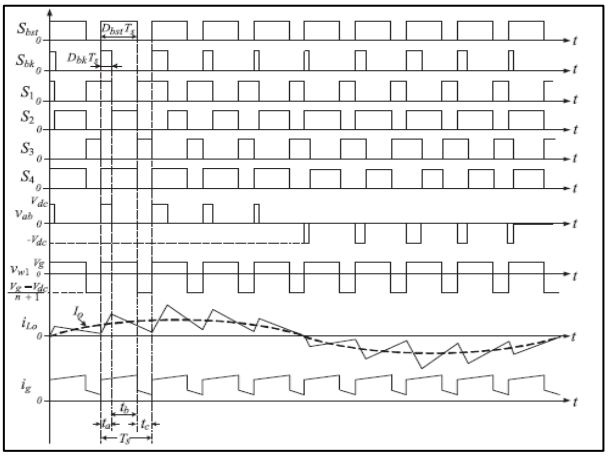

Fig. 7: Key waveforms of proposed SSBI

This paper proposes a new output filter, named the trap-CL filter, to reduce the size for ac-module applications. The trap- CL filter consists of a trap filter with a large impedance at the resonant frequency, and the CL filter. The trap filter of the proposed output filter is used to eliminate the harmonics at the switching frequency, which is dominant

in the output current. Thereby, the required filter inductance can be reduced because the CL filter handles a smaller harmonics in the multiples of the switching frequency. The proposed trap-CL filter has a maximum of −80 dB/dec. harmonic attenuation between the two resonant frequencies.

	Positive Output Voltage			Negative Output Voltage		
Switches	State A	State B	State C	State A'	State B'	State C'
M_1	ON	OFF	ON	OFF	OFF	ON
M_2	OFF	ON	OFF	ON	ON	OFF
M_3	OFF	OFF	ON	ON	OFF	ON
M_4	ON	ON	OFF	OFF	ON	OFF
D_1	OFF	ON	OFF	ON	ON	OFF
D_2	ON	ON	OFF	OFF	ON	OFF
D_3	OFF	OFF	ON	OFF	OFF	ON

Table 1: Switching States of semiconductor Devices

III. SSBI ANALYSIS AND SIMULATION

To facilitate the analysis approach, the following assumptions are adopted:

- All semiconductors are ideal with zero on resistance and voltage drop;
- The decoupling capacitor and the output filter capacitor are sufficiently large and their voltage ripple is negligible;
- Continuous current operation of both the TI and the output filter inductor is assumed.

A. Derivation of the DCM Boost Conversion Ratio

Due to changing environmental conditions, the average PV output power can drop significantly. As a result, SSBI can enter DCM of the TI. This operation regime is investigated further. In the following analysis, it is assumed that SSBI is ideal (lossless components) and that the dc-link voltage V_{dc} is regulated in closed loop to a constant value. The ac–dc power balance suggests that the ac load is reflected to the dc link and can be modeled by an equivalent dc-link resistance R_{eq}

$$R_{eq} = \frac{V_{dc}^2}{P_o}$$

Where P_o is the average power level of the SSBI. Since the principle of the dc–dc voltage step up of the proposed SSBI is similar to that of the TI boost converter, the model in Fig. 9 is appropriate for investigation of the DCM mode in SSBI. Here, the TI is modeled as an autotransformer with a moderately low magnetizing inductance Lm. Typical waveforms of the input current i_g(t) and diode current i_D(t) in the DCM are illustrated in Fig. 10, where V_{gs} is the driving signal of the switch M, i_{pk} is the peak current of the input current i_g(t) and, i_D is the average diode current. The volt–second balance of the magnetizing inductance *Lm*

Suggests

$$\frac{V_{dc}}{V_g} = \frac{(n+1)D_{bst}+D_d}{D_d}$$

B. Derivation of Voltage Conversion Ratio

Define t_a, t_b, and t_c the duration of states A, B, and C, respectively, and $T_s = t_a + t_b + t_c$ the switching period. Boost charging state, that is the time interval dedicated to charging the primary winding of the TI, takes place during states A and B whereas boost discharge takes place in state C. The total duration of the boost charging is therefore

$$t_{bst} = t_a + t_b$$

Accordingly, the resulting boost duty cycle D_{bst} is

$$D_{bst} = \frac{t_a+t_b}{T_s}$$

The dc–dc voltage conversion ratio of SSBI is

$$M_{bst} = \frac{V_{dc}}{V_g} = \frac{1+nD_{bst}}{1-D_{bst}}$$

By adjusting the turn ratio, *n*, the proposed SSBI can achieve higher conversion ratio than a traditional boost converter. According to the state description, the buck charging state, that is, the time interval dedicated to charging the output inductor, L_o , occurs in state A, whereas buck discharge takes place in states B and C while the terminals of the output filter are shorted. Thus, the duration of the buck charging is

$$t_{bk} = t_a$$

Accordingly, the resulting buck duty cycle D_{bk} is

$$D_{bk} = \frac{t_a}{T_s}$$

Clearly, under CCM condition of the output filter inductor, the voltage gain of the output section is identical to that of a buck converter and is given by

$$M_{bk} = \frac{V_o}{V_{dc}} = D_{bk}$$

Hence, the overall dc–ac voltage conversion ratio, *M*, of the proposed SSBI under CCM conditions can be derived combining

$$M = \frac{V_o}{V_g} = M_{bk}M_{bst} = \frac{(1+nD_{bst})D_{bk}}{1-D_{bst}}$$

In stand-alone application, the buck duty ratio D_{bk} is modulated to attain a sinusoidal output voltage V_o of required amplitude and frequency, whereas the boost duty ratio D_{bst} is adjusted to satisfy load power demand and so stabilize the dc-link voltage V_{dc}. An important constrain arising from SSBI principle of operation is that the buck duty ratio D_{bk} should be smaller than the boost duty ratio D_{bst} at all times: $D_{bk} < D_{bst}$.

IV. RESULT AND DISCUSSION

The single stage boosting inverter with trap-cl filter circuit was implemented in MATLAB software and the total harmonic distortion is evaluated by FFT analysis. And the closed loop Proportional Integral controller is used with Pulse Width Modulation technique.

Solar power	1 kw
Decoupling capacitor	1 mF
Linear transformer (winding 1)	V=450v, R=0.02pu, L=0.08pu
Linear transformer (winding 2)	V=550v, R=0.02pu, L=0.08pu
Diodes (D1,D2,D3)	Vf=0.8v, R=0.001ohms
Switches-Mosfet (M1,M2,M3,M4)	Ron=0.1, Rd=0.01ohms
Output Filter	L=50 mH, C=100μF
Trap-CL Filter	L=57 mH, C=47μF
Load (RL)	R=30Ω, L=30 mH

Table 2: Design Parameters

The design parameters are Vg = 60v, Solar power = 1000, Decoupling capacitor = 1 mF Linear transformer (winding 1) = V=450v, R=0.02pu, L=0.08pu, Linear

transformer (winding 2) = V=550v, R=0.02pu, L=0.08pu Diodes (D_1,D_2,D_3) = I_f =0.8v, R=0.001ohms, Switches-Mosfet (M_1, M_2, M_3, M_4)= R_{on}=0.1, R_d=0.01ohms.

This existing system consist of input solar, boost converter, voltage source inverter and output filter which is called as Two Stage Micro inverter shown in fig.6. Here the component count is high compared to Single Stage Boosting Inverter which is shown in fig.8.

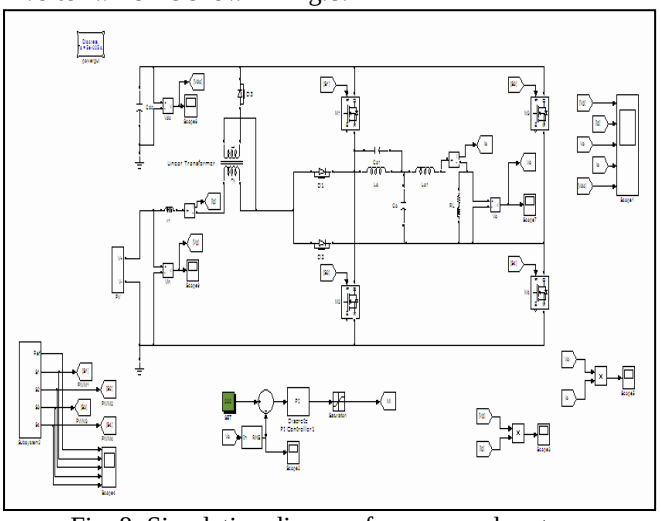

Fig. 8: Simulation diagram for proposed system

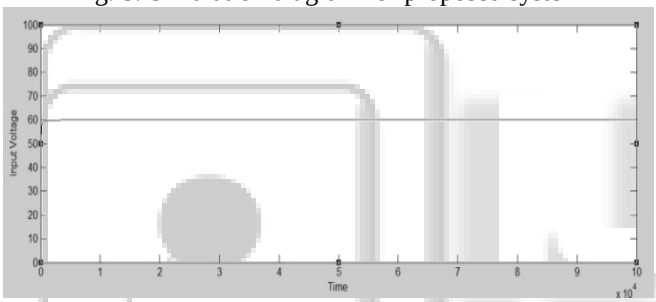

Fig. 9: Input Voltage of proposed system

The input voltage is obtained from the solar panel which is DC in nature about 60v.

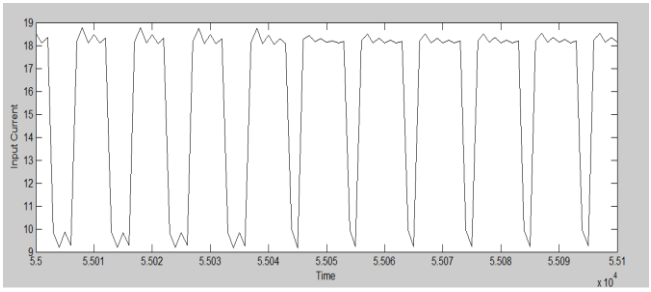

Fig. 10: Input Current of proposed system

The input voltage is obtained from the solar panel which is DC in nature about 18.5A.

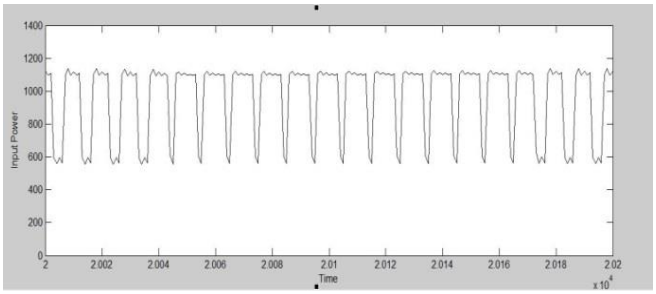

Fig. 11: Input Power of proposed system

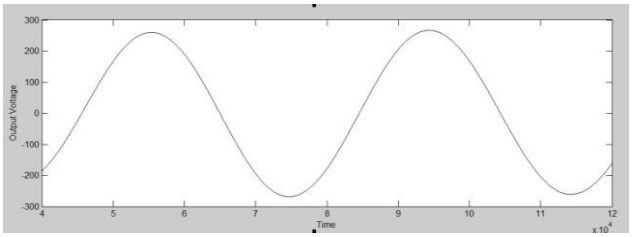

Fig. 12: Output Voltage of existing system.

In two stage or multistage system is designed to give the single phase AC output voltage of approximately 230v which is consists of boost converter, voltage source inverter and output filter. The total harmonic distortion is high compared to the single stage boosting inverter with Trap-cl filter system.

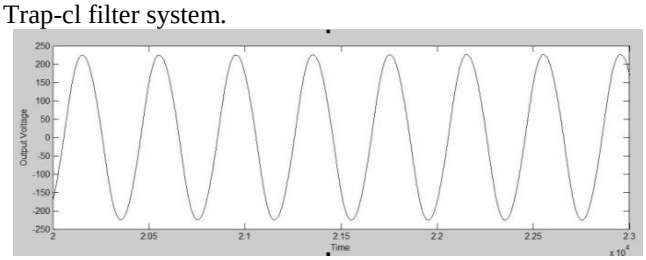

Fig. 13: Output Voltage of proposed system

The output voltage of single stage boosting inverter is in single AC voltage about 230v.

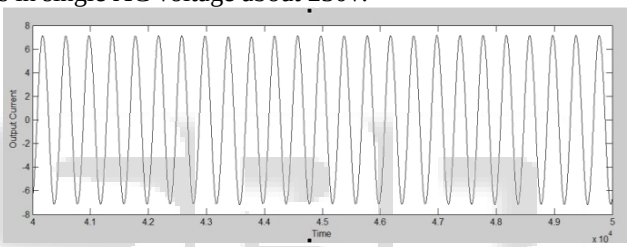

Fig. 14: Output Current of proposed system

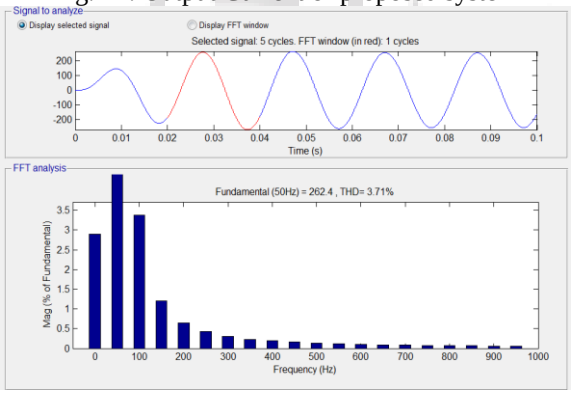

Fig. 15: THD Analysis of Two stage Inverter (Existing System)

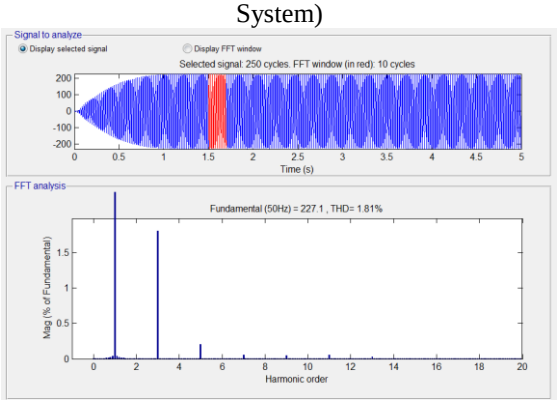

Fig. 16: THD Analysis of Single Stage Boosting Inverter with Trap-CL filter (Proposed System)

V. CONCLUSION

The single stage boosting inverter with trap-CL filter for alternative energy generation is used to reduce the Total Harmonic Distortion (THD). The proposed topology employs a TI to attain high-input voltage step-up and, consequently, allows operation from low dc input voltage. The MATLAB simulation of this paper has 60v solar input voltage. The proposed SSBI topology has the advantage of both harmonics reduction and high voltage step-up which can be further increased adjusting the TI turns ratio. By adjusting the boost duty cycle D_{bst}, the SSBI can control the dc-link voltage, whereas the output waveform can be shaped by varying the buck duty cycle D_{bk}. The OCC method was applied to shape the output voltage. In this paper, the LC resonance characteristic of a trap filter, which has large impedance at a resonant frequency, is applied to a conventional CL filter. The purpose of using the trap filter is to decrease the total filter inductance by rejecting the dominant harmonic at the switching frequency. Therefore, the output filter can be designed at a smaller size because the total harmonics are reduced. As compared to two stage inverter, the stingle stage boosting inverter with Trap-CL filter reduces the Total Harmonic Distortion from 3.71% to 1.81%.

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