Implementation of QPSK Modulator Using Direct Conversion Method

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Abstract— This paper demonstrates the design of QPSK modulator using the direct conversion architecture. Direct-conversion is different wireless receiver architecture to the well-established Super heterodyne, mainly for highly integrated, low-power terminals. The DCR gives zero intermediate frequency. The DCR data interface uses parallel data ports to transfer the data between device and FPGA processor. Bus transfers are controlled using simple hardware handshake signaling called SPI protocol. The configuration is specified using VHDL language. The QPSK modulator is designed and simulated in MATLAB 2013a and implemented using Xilinx 14.7 system generator, plan head. The output waveforms are displayed and analyzed.

Key words: QPSK Modulator, VHDL, FPGA

I. INTRODUCTION

In wireless communication systems the modulators are the basic requirement and they are designed to ease the channel distortion & to utilize in RF communication, hence various category of carrier modulation techniques has been already anticipated according to channel properties & data rate of the system. QPSK (Quadrature Phase Shift Keying) is one of the modulation scheme and it has the ability to transmit twice the data rate for a given bandwidth and it is used in wireless communication system.

The AD9364 is a RF transceiver which is utilized *direct* conversion receiver to summarize the QPSK modulator. The AD9364 is an exceedingly coordinated radio frequency (RF) transceiver robust for being arranged for an extensive variety of utilizations. The device coordinates all RF, mixed signal, and digital blocks important to give all transceiver capacities in a solitary device. The AD9364 information interface utilizes parallel information ports (P0 and P1) to exchange information between the device and the FPGA.

The super heterodyne implementation of a multimode receiver requires multiple filters that not only increase the production cost but also the physical dimension of the handset. Thus, super heterodyne receiver is not a practical topology for multimode receiver design.

To overcome the issues in super heterodyne the direct conversion architecture is used and it is suitable for multimode receiver design.

It performs a single frequency conversion and reduces the basic circuit complexity. The conversion of the modulated signal to base band is done in a single frequency conversion. This avoids the complexity of the super heterodynes two or more frequency conversions IF stage and image rejection issues.

II. BLOCK DIAGRAM

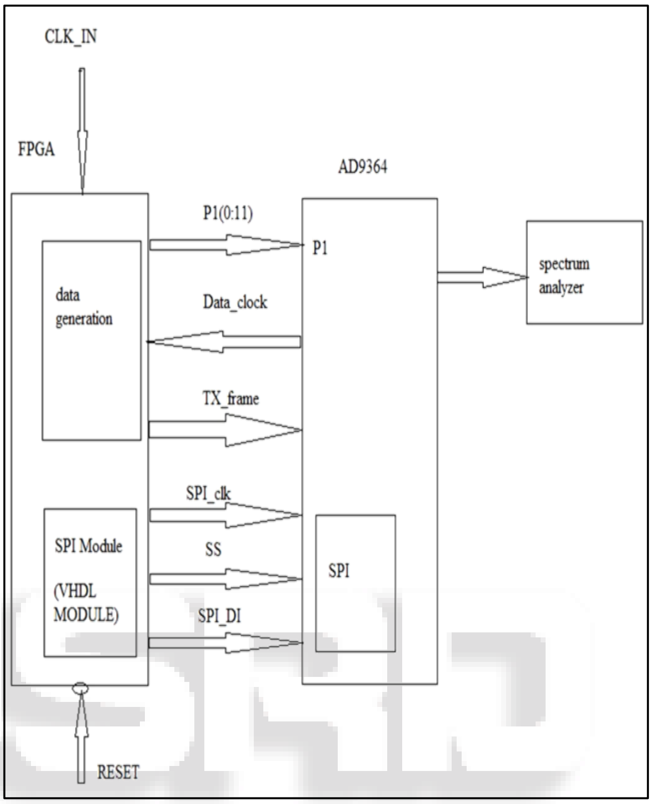

Fig. 1: Block Diagram

The AD9364 data interface make use of parallel data ports (P0 and P1) to relocate data among the device and the BBP. The data ports can be configured in either single-ended CMOS format or differential LVDS format. Bus transfers are controlled using simple hardware handshake signaling called SPI protocol. The two ports can be operated in either bidirectional (half-duplex) mode or in full duplex mode.

III. METHODOLOGY

The below diagram demonstrates the Xilinx System Generator’s blocks in the design and generate a synthesizable design which can be implemented using Xilinx ISE’s Project Navigator.

System generator generates HDL netlist for the QPSK design by selecting ARTIX7 FPGA family. This HDL netlist is invoked to the TOPMODULE instantiation written in VHDL modeling language. Inturn TOP MODULE contains the register configuration of AD9364 for 400Mhz. In order to configure the AD9364 device and FPGA processor, the pin assignment has to be done by creating UCF constraint file.

The UCF file contains the pin assignment for inputs and outputs used in the port instantiation in top module. Once the FPGA is ready with the UCF files it has to be synthesized for the functionally. If this successfully executed it undergoes to the translate, mapping, place and routing to verify the static timing utilization. After verifying it generates the BIT FILE. This bitfile is used for the real time verification of the design in FPGA. Experimental results are reported and mapped onto the Xilinx ARTIX-7 FPGA.

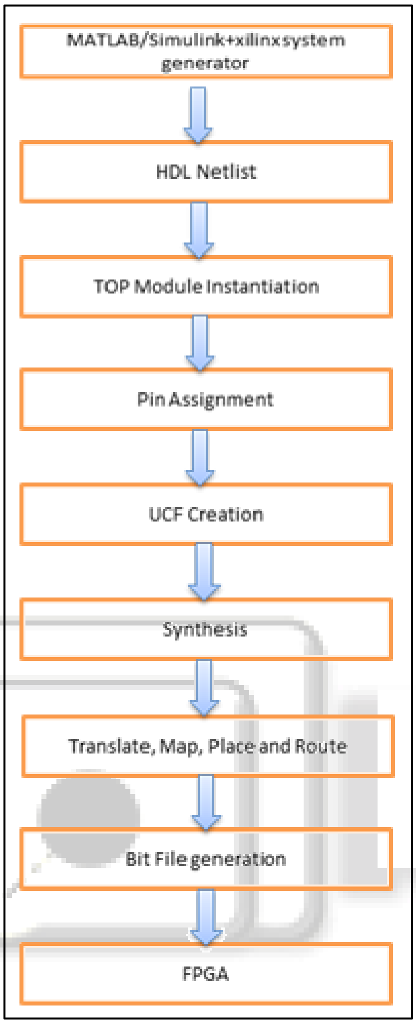

Fig. 2:

IV. DESIGN OF QPSK MODULATOR IN SYSTEM GENERATOR

The figure illustrates the implementation of a QPSK Modulator using System Generator tools in Simulink.

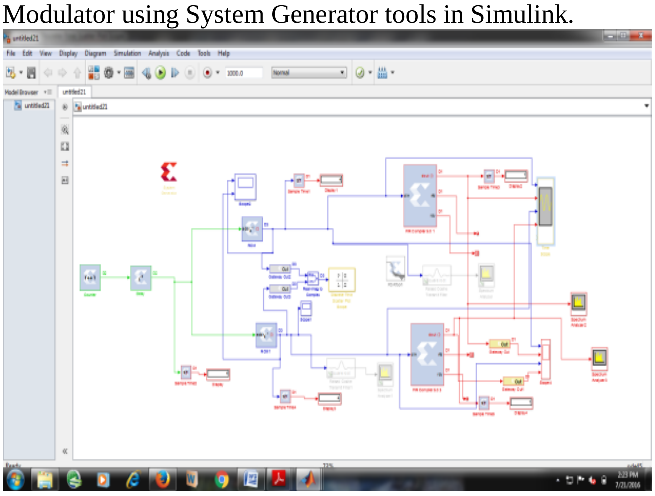

Fig. 3: design of QPSK using RRC filter

The QPSK modulator maps the four signals and it generates the two symbols at a time. These four symbols are mapped in costellation diagram. The four symbols are (0.707+j0.707), (0.707-j0.707),(-0.707 +j0.707), (-0.707-j0.707). These symbols are separated in to I phase and Q phase. The real numbers are stored in ROM in the I channel and imaginary values are stored in ROM in the Q channel. These values are filtered by using root raised cosine filter (RRC), it provides the smoothness of the signal.
System clock generated with the frequency of 10 MHz.

A. Constellation Diagram

this diagram codes four symbols are illustrated in scatter plot.

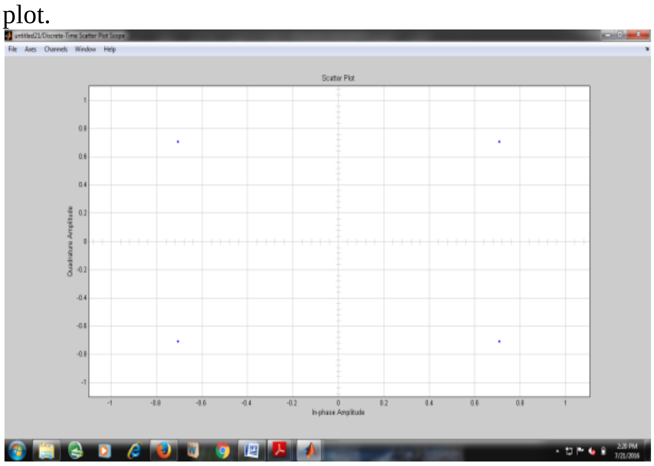

Fig. 4: scatter plot of QPSK

B. Output Waveform

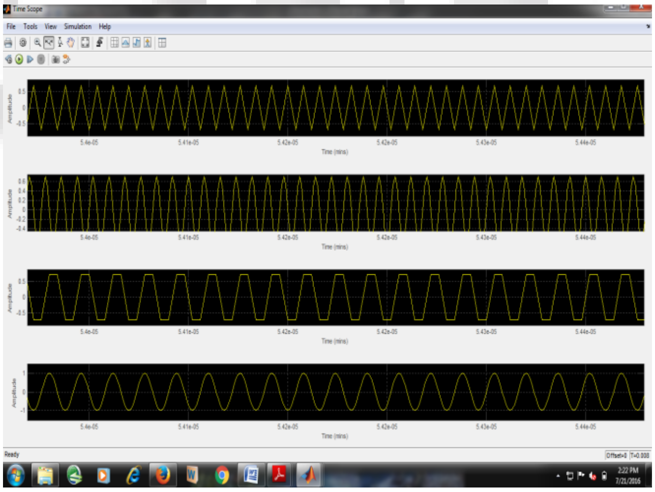

Fig. 2: Output of RRC filter

C. FPGA Implementation

The output files in the synthesis are required in Xilinx ISE software are in the form of EDIF (Electronic Design Interface File) and UCF (User Constraints File) formats. This represents the optimized netlist for integrated design, timing constraint and FPGA pin assignment respectively. . To implement the synthesized design into Artix-7 FPGA development board, Xilinx ISE performs steps such as Translate, Map, Place & Route (PAR), Bit Generation, and Program Download to FPGA for the QPSK model. Make sure no errors for each step described above.

Due to no error and warning for DRC (Design Rules Checker) and bit-stream generation process, the configuration bit-stream file is downloaded to Artix-7 FPGA board. The ADC input and DAC output signals for the QPSK transmitter is connected to spectrum analyzer in order to display real-time result.

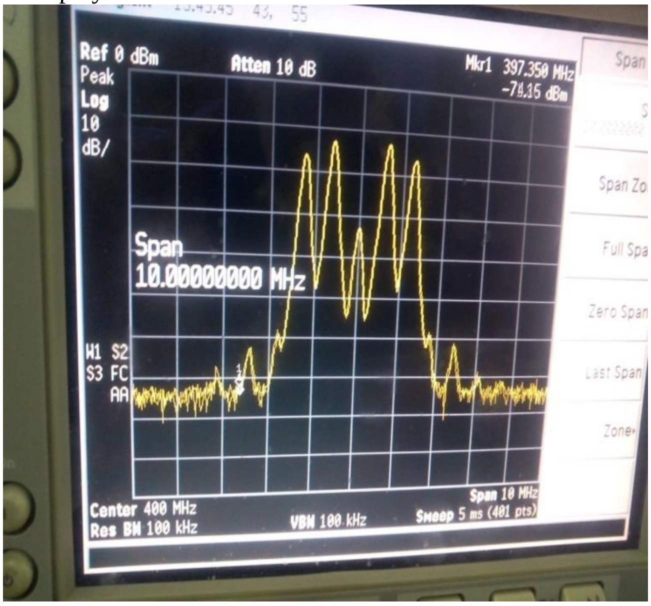

Fig. 5: Output of QPSK modulator in CRO

V. Conclusion

This paper presents the theoretical analysis and simulation of QPSK modulator in MATLAB 2013a, system generator. QPSK is mapped to FPGA using direct conversion method. The AD9364 is broadly used in 3G and 4G base station applications and it has a high performance, extremely integrated radio frequency (RF) Agile Transceiver. The AD9364 operates in the range of 70 MHz to 6.0 GHz.

The implementation result shows the output of QPSK transmitter in frequency domain for 400MHZ.

Future work includes the design of QPSK demodulator using AD9364 method and with the register configuaration of 400Mhz.

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