Low Power Dual Edge Triggered Flip Flop using Multi Threshold CMOS
a Review

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Abstract— In the present work, a low power dual edge triggered flip flop design using multi threshold CMOS is proposed. Proposed Flip-Flop (FF) has three main changes. First, the pulse generation control logic is designed with EXOR gate and inverter chain which reduces the complexity and extra switching in pulse generator circuit. Second, signal feed through technique with some modification is devised to speed up the charging and discharging along the critical path only when needed. Third, multi-threshold CMOS technique is also applied to get low power dissipation. As a result, no. of transistors in pulse-generation circuit has been reduced for power and area saving. Various post layout simulation results based on CMOS 90-nm technology reveal that the proposed design features the best power-delay product performance in all FF designs under comparison.

Key words: Flip-Flops, pulse triggered, low power, signal feed through technique, FF with minimum transistors

I. INTRODUCTION

The last decade has seen the rapid growth in battery operated portable systems like smart cellular phones and palm-top computers used for personal communication services. Since these systems are dedicated to multimedia, they are designed not only for low power consumption but also for higher signal or data processing capabilities. Hence design of low power and high performance VLSI systems have become necessity for the modern designers [1]. In a VLSI system, the clock subsystem comprising of the clock interconnection network and timing elements (flip-flops and latches) is one of the most power consuming component [2][3]. In the clocking subsystem, the design of energy efficient flip-flop (FF) is a major concern. As a result, reducing the power consumed by flip-flops has a deep impact on the total power consumed. The most commonly used flip-flops in contemporary microprocessors are master slave and pulse-trigger flip-flops [3]. The pulse-triggered flip-flops are more popular than the conventional master slave flip-flops because of their single-latch-structure and better power efficiency. Pulse-triggered FFs are classified into two types, implicit pulsed (pulse generator is the part of the latch) and explicit pulsed (pulse generator and latch are separate) [4]. There are some other approaches for FFs design such as semi dynamic, sense amplifier based and hybrid latch based [5]. A pulse flip-flop (PFF) design consists of an explicit pulse generator and a latch where pulse generator is used for strobe signals and latch is used for data storage. Conventional single-edge-triggered flip-flops (SETFF) are designed by cascading two oppositely phased latches and are active either on rising or falling edge of the clock. Double-edge-triggered flip-flops are preferred over single edge because of its advantage that they operates at half of the clock frequency while maintaining the same data throughput compared to SETFF or we can say double-edge-triggered flip-flops requires a lower clock frequency to achieve comparable performance [6]. In the conventional CMOS based digital circuits there are mainly three types of power consumptions: (i) switching power, (ii) short-circuit power, and (iii) leakage power. The main sources of leakage power are as follows: sub-threshold leakage, gate-oxide leakage, gate-induced drain leakage (GIDL) and reverse bias junction leakage. Sub-threshold leakage dominates over the all leakage currents. Sub-threshold leakage power is reduced by using a high threshold voltage in some part of the design or circuit. Higher threshold voltage is achieved either by adjusting the channel doping concentration or by applying a body bias. This technique is known as MTCMOS. The unique feature of MTCMOS is that it uses both high and low-threshold voltage MOSFETs in a single chip [7]. In the present work, a low power dual edge triggered flip-flop using MTCMOS is proposed.

II. LITERATURE OVERVIEW

A. Dual Edge Triggered Conditional Discharge FF

Fig. 1 (a) shows dual edge triggered conditional discharge FF (DCDFF) with CLK pulse generator (CLKPG) [8]. CLKPG uses two transmission gates (TG) for generating CLK pulse (CP) at the rising and falling edge of the CLK. In the latch, assume Q is previously “0”, so Qb is “1”. When Data is “1”, then CLK is “0”, then CP is also “0” which turn ON the transistor P1 and charges the node X to “1”. When CP occurs, then transistor N3 is ON that discharges node X through transistors N1, N2 and N3 to ground. It turns ON the transistor P3 which charges output node Q to “1”. When Data is “0” and CP occur, then output node Q discharges through transistors N4 and N5. It means input Data is transferred to output Q at the occurrence of CP (either rising or falling edge). But it dissipates more power at input stage when input Data is low.

![Image](a)
Dual edge triggered static pulsed FF (DSPFF) with its CLKPG is shown in Fig. 1(b) [9], [10]. In CLKPG, 4 inverters chain is used to generate delay in the CLK. These delayed versions are used to generate sampling window around the positive edge and negative edge of CLK with the help of two pass transistors N1 and N2. In latch circuit, inputs are applied to the SB and RB lines directly through two pass transistors N5 and N6 controlled with clock pulse (CP). Two PMOS transistors with two weak NMOS transistors are used to avoid the floating of SB and RB nodes. Due to static nature of DSPFF, it eliminates unnecessary transitions which reduce power consumption in the flip-flop (FF). DSPFF consumes large power consumption because of large leakage current. Symmetrical output delays can be obtained by adjusting transistors' aspect ratio.

III. PROPOSED FF DESIGN

Here, we already described some dual edge triggered FF which has more power dissipation during internal node X discharging. So, we remove this problem by connected P1 gate to CLK pulse Z which almost turn OFF P1 transistor during the discharging of internal node X. Signal feed through technique [11] has the advantage of faster switching (charging and discharging) of output node Q and low power dissipation than other techniques. Dual edge triggered FF has lower power dissipation than single edge triggered FF because of half CLK frequency at the same time. If we apply Multi threshold CMOS technique with dual edge triggering, it lowers leakage power dissipation as well as overall power dissipation [12]. MTCMOS reduces the static leakage power (sub-threshold leakage) dissipation. So, here we used Signal feed technique with dual edge triggering using MTCMOS. We know that MTCMOS uses sleep transistors with high threshold for low power dissipation but we apply MTCMOS directly at charging and discharging transistors for low leakage instead of extra sleep transistors. Fig. 2 shows the representation of low threshold and high threshold transistor for MTCMOS technique.
Here, we used Signal feed through FF with three changes [11]; first, we apply CLK pulse at gate of transistor P1 by removing ground from gate terminal; second, we use MTCMOS technique; and third, we remove one inverter from the output of FF for getting Qbar. Number of transistors in Signal feed through FF and proposed FF are same but proposed FF has lower power dissipation and delay with respect to Signal feed through FF. When CLK=0, then no CLK pulse is generated but it charges intermediate node X through transistor P1. Assume output Q is initially “0”, so Qbar is “1”. If the input Data is “1”, then node X is discharged with the occurrence of CLK pulse Z. It will start charging node Q through transistor P2. But at the same time, transistor N4 is ON with the CLK pulse, that also charges (or give push) to the node Q because node Q is directly connected to the input Data through transistor N4. And when Data becomes “0”, then node X doesn’t discharge, but with the occurrence of CLK pulse, node Q discharges through transistor N4 to the input Data instantly.

IV. SIMULATION RESULTS

DCDFF and DSPFF (described in Section II) and proposed FF (described in Section III) are simulated for the better performance. All simulation results are evaluated at 90nm CMOS process technology using Tanner EDA with 1V power supply. CLK frequency used in proposed FF (dual edge triggered) is 250MHz but this frequency is similar as 500MHz CLK frequency used in single edge triggered FFs. FFs are loaded with 20fF capacitance at the output. Conventional FFs are simulated with 0.18V threshold voltage, but proposed FF used 0.18V and 0.36V threshold voltage. Fig.6. Shows the simulation waveform of proposed dual edge triggered FF.

![Fig. 5: EXOR based CLK pulse generator](image)

**Table 1: Performance Comparison**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>DCDFF</th>
<th>DSPFF</th>
<th>Proposed FF</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of Transistors</td>
<td>28</td>
<td>20</td>
<td>24</td>
</tr>
<tr>
<td>Min. D-to-Q Delay (ps)</td>
<td>155.79</td>
<td>132.44</td>
<td>99.73</td>
</tr>
<tr>
<td>Power (100%) uW</td>
<td>31.02</td>
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<td>Power (25%) uW</td>
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<td>Power (0%-all 1) uW</td>
<td>13.71</td>
<td>14.10</td>
<td>12.94</td>
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<tr>
<td>Power (0%-all 0) uW</td>
<td>12.80</td>
<td>11.42</td>
<td>10.09</td>
</tr>
</tbody>
</table>

Table 1: Performance Comparison

Here, Table 1 shows the performance comparison of proposed FF with MTCMOS and without MTCMOS with signal feed through technique. It is clearly noticed that proposed FF with MTCMOS has highest performance and low leakage power dissipation.

V. CONCLUSION

This paper presents the low power dual edge triggered FF using MTCMOS technique with better simulation results at 250MHz CLK frequency, 1V power supply and 90nm CMOS process technology. MTCMOS uses MOSFET’s with two different threshold voltages (Low-threshold and High-threshold) on a single chip. Low-threshold voltage MOSFET’s improving the speed performance at a low supply voltage of 1 V, while high-threshold MOSFET’s suppress the standby power dissipation. Obtained results shows low D-to-Q delay, lower power dissipation than previous single edge triggered FF. Additionally, proposed FF has 57.4% power saving at 100% switching activity than other dual edge triggered FF.

REFERENCE


