

# Implementation and Simulation of a Differential Amplifier using Dual Gate Organic Thin Film Transistor

Shilpa Saini<sup>1</sup> Yogendra Saini<sup>2</sup>

<sup>1</sup>Uttarakhand Technical University, Dehradun, India <sup>2</sup>National Institute of Technology, Uttarakhand, India

**Abstract**— In modern IC amplifiers an essential building block is the differential amplifier. Many electronic devices internally use differential amplifiers. There is a type of electronic amplifier is differential amplifier that multiplies the difference between two inputs by some constant value and this constant value is called differential gain. In this paper we propose a differential amplifier implemented using dual gate organic thin film transistors (OTFTs). P-type pentacene dual gate OTFT structure is used to design amplifier device. Implementation and simulation of device is done using industry standard Atlas (Silvaco) 2-D device simulator. Results show that the amplifier has well behaved large signal characteristics and good linearity for inputs between -1 and 1 V.

**Key words:** OTFT, Dual Gate, Differential Amplifier, Pentacene

## I. INTRODUCTION

A thin film transistor (TFT) is a unique type of FET realized by depositing a semiconductor active layer, thin metallic films for the contacts, and a dielectric layer. The electrical performance of a TFT is depends highly on the semiconductor material, as the electric current flows through the semiconductor layer is closer to the dielectric interface so the electric characteristics of a TFT determine by the properties of the semiconductor layer and the dielectric interface. Electrical behaviour of Source and drain contacts are another factor that influences TFT performance. Charge carriers are injected into the semiconductor through source contact and charge carriers are extracted through the drain contact. In TFT, mostly used material for semiconductor layer is hydrogenated amorphous silicon, polycrystalline silicon and organic semiconductors. The major difference between TFTs and MOSFETs is that while a TFT is an insulated gate device, it doesn't works in inversion region, it works in accumulation region. In TFT, mostly used materials for semiconductor layer are hydrogenated amorphous silicon, polycrystalline silicon and organic semiconductors. Among these, organic semiconductors are mainly suitable for solution-processing or vacuum-deposition at or near room temperature. In the last twenty years, the attention in organic electronics has been constantly growing. This technology has made lots of development both from the reliability and the performance point of view, enabling the design of progressively more complicated organic circuits. Digital circuits, like RFID transponders and microprocessors have been demonstrated in organic electronics. Recently, organic electronics have become a hopeful technology for different applications required low cost, large area coverage, flexible substrate, and low temperature processing. . The most important module of the organic electronics is organic thin film transistor (OTFT) that is basically a field effect transistor (FET) uses organic semiconductors and organic dielectrics. OTFTs have many advantage as, it can be realize on flexible

substrates at room temperature, low cost, mechanically flexible, and large area electronics applications. These properties of OTFT allow it for their use in different merging application fields, such as in electronic paper or in flexible displays [1], in sensors [2], and in low-cost radiofrequency identification cards (RFIDs) [3, 4]. The limitation of organic material is low mobility due to this where is fast response (ns) speed and low size (nm) are required in electronic applications they are not allowed, but some application where slow responses of OTFT are accepted: for example smart tag, displays, photovoltaic, radio-frequency identification (RFID) circuitry, and chemical sensor. Over the last two decades, OTFTs device performances have improved dramatically. The pentacene based OTFTs have the superior performances as high field effect mobility and large on/off current ratio. Other issues of the practical OTFTs that should be improved are the improvement of passivation performance and the control of electrical parameters such as threshold voltage ( $V_{th}$ ) and on-current. These problems can be solved using dual-gate OTFT structure and it has different bias configuration and offers higher flexibility. The design of OTFTs circuits is basically use same steps as the silicon technology. Till the moment OFETs are normally P type transistors although N type OFETs have been reported during the last years [5, 6], but N type OTFTs suffer from low carrier mobility then P type OTFTs, process complexity, and stability problems. As in FETs CMOS technology is used, in OTFTs Ambipolar OFETs are used but they suffer from the hysteresis. So in this paper pentacene based p-type dual gate otft device is used. For simulation of dual-gate OTFT industry standard Atlas (Silvaco) 2-D device simulator is used.

## II. DIFFERENTIAL AMPLIFIER

In modern IC amplifiers an essential building block is the differential amplifier. Many electronic devices internally use differential amplifiers. There is a type of electronic amplifier is differential amplifier that multiplies the difference between two inputs by some constant value and this constant value is called differential gain. An ideal differential amplifier output is given by:

$$V_{out} = A_d(V_{in}^+ - V_{in}^-) \quad (2.1)$$

Where  $V_{in}^+$  and  $V_{in}^-$  are the input voltages and  $A_d$  is the differential gain of amplifier. If  $V_{in}^+$  and  $V_{in}^-$  are equal then the output may not be zero as it should be for the ideal case. Thus for a practical amplifier output expression needs to include another term and this is given by:

$$V_{out} = A_d(V_{in}^+ - V_{in}^-) + A_c((V_{in}^+ + V_{in}^-)/2) \quad (2.2)$$

Where,  $A_c$  and  $A_d$  is the common mode gain and the differential mode gain of the amplifier, respectively.

## III. DIFFERENTIAL AMPLIFIER BASIC PRINCIPAL

In differential amplifier it is desirable to cancel out bias voltages and noise that appear on both inputs thus a low common-mode gain is generally considered good. The ratio

between differential-mode gain and common-mode gain is called common-mode rejection ratio and it defines the amplifier efficiency of refusing voltages effectively that are common to both inputs from affecting the output. Common-mode rejection ratio (CMRR) is given by

$$CMRR = A_d/A_c \quad (3.1)$$

In a perfect symmetrical differential amplifier,  $A_c$  is zero and the CMRR is infinite. A differential amplifier is used more often than the single input one, when one input of the differential amplifier is grounded it is called a single ended amplifier, a single ended amplifier used less often than the differential amplifier. Basically an operational amplifier is a differential amplifier having a very high differential-mode gain with very high input impedances and rather low output impedance. Sometimes some types of differential amplifiers are formed by connecting smaller differential amplifiers with other components. [7, 8] differential amplifiers are use as the input amplifier stage in many analog circuits. The input amplifier stage is supposed to have the high input impedance, large common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR), much of the op-amps voltage gain and noise and low dc offset voltage. The circuits operate in a differential mode; can provide high differential gain along with low common-mode gain and therefore a large CMRR. The differential configuration also provide a large PSRR, as variations of VDD are to a large extent are cancelled in the differential output voltage  $V_{O1} - V_{O2}$ .

In differential amplifier for appropriate operation all transistors including the one forming the current source are considered to operate in saturation. In an ideal differential amplifier the two input nodes are considered to have same resistance. We assume that the differential pair is matched and the current source "I" is ideal, i.e., its internal conductance  $\bar{g}$  is zero. The differential gain of differential amplifier is the same as for a simple inverter; on the other hand the stage provides also a rejection of noise in the power supplies (VDD, VSS) and common-mode signals, all of which are cancelled out by the differential operation of the stage. To calculate the gain of the differential amplifier circuit the low frequency small signal equivalent circuit of the differential amplifier stage can be used. The gain of the differential amplifier circuit is expressed as

$$A_v = g_m R_D \quad (3.2)$$

Here  $g_m$  defines the transconductance of the transistor.

The differential pair is basically as two single transistor amplifiers in parallel to allow it the capability to reject disturbing common mode signals and hence it is the basis of all fully-differential circuits. In DC operation of the differential amplifier when the voltage is same at the gate of both transistors in the differential pair that means they both operate with the same  $V_{gs}$  hence they both transistors have the same current. While the current source fixed the sum of the currents flowing through them and current in each transistor should be " $\frac{I_{SS}}{2}$ " and we assume that the voltage drop is same across the two PMOS transistors and therefore the voltage is same at the two output terminals of the differential amplifier. Accordingly for zero differential input we have zero differential output. Now consider if the gate voltage of left pmos increases by  $V$  and the gate voltage of right pmos decreases by  $V$ . Now if increase the gate voltage

of any one transistor means the current flowing through it should be increase but the sum of current is fixed flowing through the both transistors of the differential pair and equal to  $I_{SS}$  so as increase the current in one transistor the current in other transistor decrease by the same amount. Let this change in current  $I_C$  can be given by

$$I_C = g_m \frac{V_{gs1} - V_{gs2}}{2} \quad (3.3)$$

Where,  $(V_{gs1} - V_{gs2})$  defines the differential input.

The output of the two output transistors in differential amplifier can be given by

$$V_{O1} = V_{eq} + i_c R_d \quad (3.4)$$

$$V_{O2} = V_{eq} - i_c R_d \quad (3.5)$$

Therefore the differential output is

$$V_{od} = 2i_c R_d \quad (3.6)$$

Thus the gain can be given by

$$A_{d,m} = ((V_{O1} - V_{O2}) / (V_{gs1} - V_{gs2})) \quad (3.7)$$

$$A_v = -g_m R_D \quad (3.8)$$

Fig.1 shows a schematic diagram of the OTFT differential amplifier gain block using only p-type transistors. Devices  $M_1, M_2$  comprise a differential pair and  $M_3, M_4$  are active loads connected to source at  $-7$  V and drain connected to gate. Where,  $M_5$  operates as a current source providing bias current to the differential pair. Supply voltages are  $+10$  V and  $-7$  V, and input common-mode voltage is at ground (0 V) used for differential amplifier.

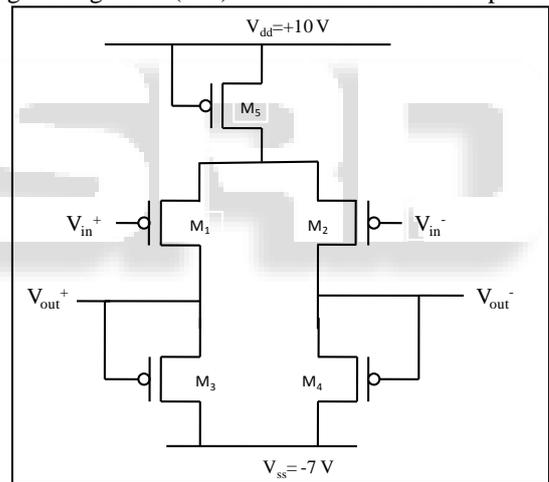


Fig. 1: Schematic diagram of OTFT differential amplifier gain block with dc bias voltages.

#### IV. SIMULATION RESULTS OF DIFFERENTIAL AMPLIFIER

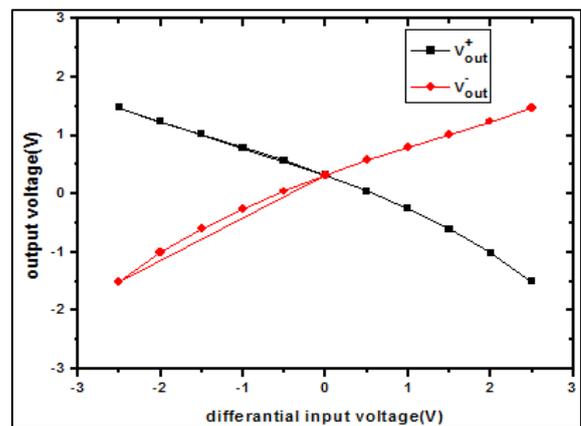


Fig. 2: differential output voltage for a differential input swept again from  $-3$  to  $3$  V.

Fig.2 shows dc analysis of simulated signal voltages for the differential amplifier for a differential input swept from -3 to 3 V at a common-mode input voltage level of ground. These results show that at a time the both outputs are inverted to each other. All devices are reliably in saturation, operating at drain source voltages above their drain-source saturation voltages ( $V_{DS} > V_{DSAT}$ ). The supply voltages for differential amplifier are +10 V and -7 V and common mode input voltage is 0V. The amplifier has well behaved large signal characteristics and good linearity for inputs between -1 and 1 V. The input offset voltage is 0V and the simulated differential dc gain is +1.87 (~2). Transient response for differential amplifier is shown in fig.3.

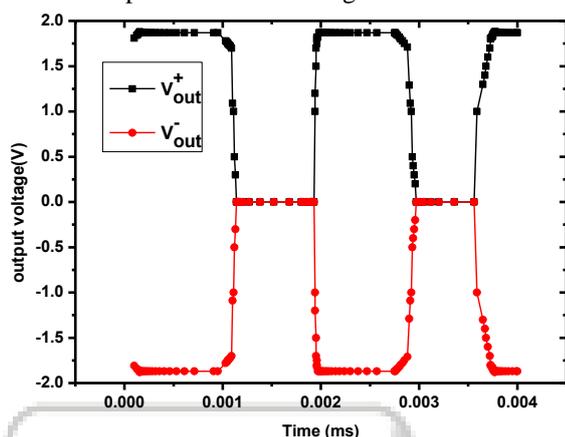


Fig. 3: Transient Analysis of differential amplifier.

## V. CONCLUSION

In this paper we simulated a pentacene otft differential amplifier circuit. We have also discussed basic working principle and simulation results of differential amplifier. Simulation result of amplifier is presented. Differential amplifier simulation results give the differential dc gain about +1.87.

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