Design of High Performance Compressor based Urdhwa Tiryakbhyam Multiplier

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Abstract— In the new technology of VLSI, Communication and signal processing. there is an vast demand for the high speed and low area design. In this project we have designed compressor based multiplier, We introduced 4:2 Compressor replaced several half adder and full adder then reduced the complexity of circuit and addition to that by using vedic mathematics. There are 16 sutras in vedic multiplication in which "Urdhawa Tiryakbhyam" has been noticed to be the most efficient one in terms of speed. The multiplier is coded in VHDL and synthesis and simulation by using Xilinx ISE 13.1. Further the design multiplier compared with proposed multiplier in terms of delay and area.

Key words: High Speed Multiplier, 4:2 Compressor, Vedic Mathematics, VHDL Code

I. Introduction

The Digital signal processing we have to perform operations like frequency domain filtering (FIR, IIR) and frequency transformation. Multiplication is an essential hardware component for this operation. Performance of the multiplier is heart of element in determining the performance of the entire system. In this system the multiplier is the slowest and most time consuming element. Thus the optimization of the multiplier speed and area is a major challenge for the system designers. This challenge and drawbacks can be successfully overcome by the use of 4:2 compressor based multiplier.

The proposed multiplier incorporate a compressor based technique to increase the speed of Vedic mathematics based Multiplier. 4:2 Compressors replaced several Full adder and Half adder in this multiplier. Compressor can add more than three bits at a time and computes the operation with fewer numbers of gates and has higher speed as compared to full adder. Since the compressor uses few gates so area of compressor reduces in comparison to equivalent full adder circuit. Area optimization and performance of Multiplier is the main domain of concern in the field of VLSI Design. The speed of processor depends on the performance of Multiplier.

II. Vedic Mathematics

Swami Bharati Krishna Tirthaji (1884-1960), rediscovered aset of 16 Sutras (aphorisms) and 13 Sub - Sutras (corollaries) from the Atharva Veda. He developed unique methods and techniques for amplifying the principles contained in the sutras and their sub-sutras, and coined the term Vedic Mathematics. The Sutras apply to and cover almost all operations in Mathematics. Even we can apply to get the solution for large number of mathematical operations. Benefits of the Sutras save a lot of time and effort in solving the problems. In Vedic mathematics, two sutras are dedicatedly used for multiplication functions. One is Nikhilam Navatascaramam Dasatah sutra and other is Urdhva–Tiryagbhyam sutra. Our focus is only on the Urdhva–tiryagbhyam sutra as in the Nikhilam Navatascaramam Dasatah sutra, multiplier and multiplicand both are required to be nearer to bases of 10, 100, 1000 that is increased powers of 10. The sixteen sutras of Vedic mathematics and their meaning are listed in Table 1 [11]

Ekadhikena Purvena By one more than the	Ekadhikena Purvena By one more than the
Nikhilam Navatascaramam Dasatah	All from 9 and last from 10 (Multiplication)
Urdhva – Tiryagbhyam	Vertically and crosswise (Multiplication)
Parvartya Yojayet	Transpose and adjust (Division of polynomial equation)
Sunyam Samyasamuccaye	When the sum is the same that sum is zero
(Anurupye) Sunyamanyat	If one is in ratio, the other is zero
Sankalana yavakalanabhyam	By addition and by subtraction
Puranapuranabhyam	By the completion or non-completion
Yavadunam	Whatever the extent of its deficiency
Vyastisamastih	Part and Whole
Sesanyankena Caramena	The remainders by the last digit
Sopantyadvayamantyam	The ultimate and twice the penultimate
Ekanyunena Purvena	By one less than the previous one
Gunitasamuccayah	The product of the sum is equal to the sum of the product
Gunakasamuccayah	The factors of the sum is equal to the sum of the factors

Table 1: Sixteen sutras of Vedic mathematics [11]

A. *Urdhwa Tiryakbhyam Sutra*

The Urdhwa Tiryakbhyam Sutra is one of the most highly preferred algorithms for performing multiplication. The algorithm is competent enough to be employed for the multiplication of integers as well as binary numbers. The term "Urdhwa Tiryakbhyam" originated from 2 Sanskrit words Urdhwa and Tiryakbhyam which mean "vertically" and "crosswise" respectively. The main advantage of utilizing this algorithm in comparison with the existing multiplication techniques is the fact that it utilizes only logical "AND" operations, half adders and full adders to complete the multiplication operation and saving a lot of processing time.

1) The Following steps in Urdhwa- Tiryakbhyam sutra

- Step 1: Start form right and multiply vertically from right only
- Step 2: Multiply cross only bit by bit from right to left and them along with carry form previous step
- Step 3: Finally multiply vertically from left only and add the previous carry

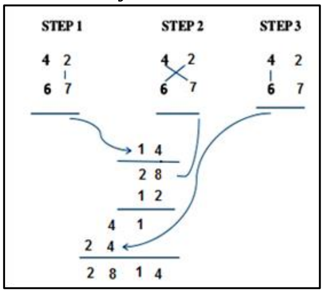

Fig. 1: Multiplication of Two Decimal Numbers Urdhawa Tirayakbhyam Sutra

B. Vedic Multiplier (Urdhwa-Tiryakbhyam)

- The Vedic multiplier operating speed is higher as compare to array and booth multiplier.
- It is very less delay as compared to another multiplier.
- It is take less complexity as compared to another multiplier.
- FPGA implementation is most efficient.
- It is both side operand unsigned and signed.
- It is regular structure.
- It is consume less power.

III. 4:2 COMPRESSOR

The 4:2 compressor has 4 input bits and 1 previous input produced 3 output bits (Sum, Carry, Cout), Cin = 0 at the initial stage. Cout send towards the next steps. The output represent sum of the five input so it is really a 5 bit adder. Avoid carry propagation the value of Cout depends only on IN0, IN1, IN2 and IN3. It is independent of Cin.

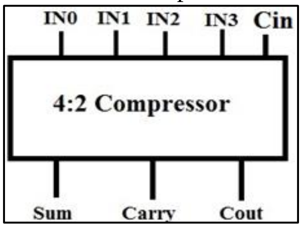

Fig. 2: Basic diagram of Compressor 4:2

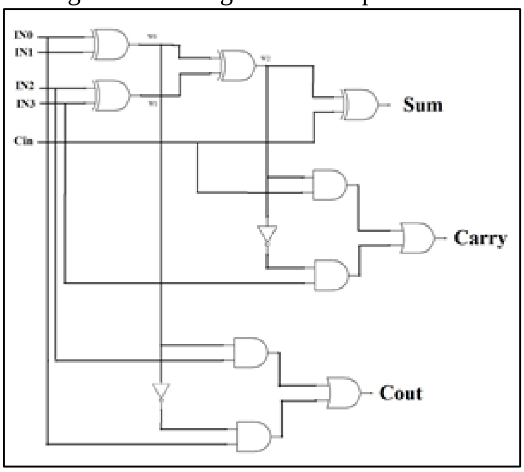

Fig. 3: Gate level Diagram of 4:2 Compressor

1) Equations

Sum = W2 xor Ci

Carry = (W_2 and C_{in}) Or (Not W_2 and In_3)

Cout = (W_0 and In_2) Or (Not W_0 and In_0)

IV. IMPLEMENTATION OF URDHAWA-TIRYAKBHYAM MULTIPLIER

The multiplier structure is divided into three stages:

- Partial Product generation stage.
- Partial Product addition stage.
- Final addition stage.

A multiplier consists of two operands, multiplicand "Y" and a multiplier "X". In the first stage, multiplicand and multiplier is multiplied bit by bit to generate the partial products. The second stage is very important add these partial products. And third stage is including ripple carry adder then get a result of multiplier. The hardware structure of the 4:2 compressor based urdhwa-tiryakbhyam multiplier. The 16x16 bit input of multiplier and got result is 32 bit, compressor replaced several half adder and full adder. The following fig:4 shows the external structure multiplier and we see the three stages in the structure and the fig:5 shows a 4:2 compressor structure.

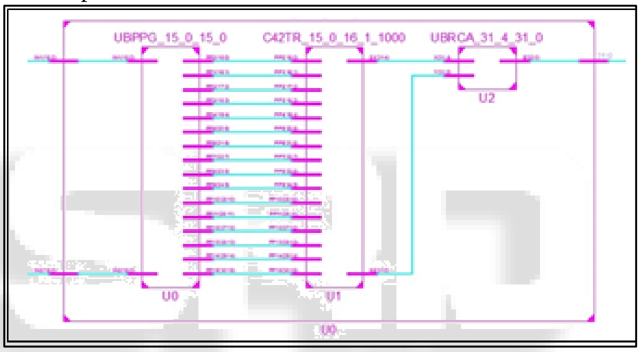

Fig. 4: Top level entity of multiplier

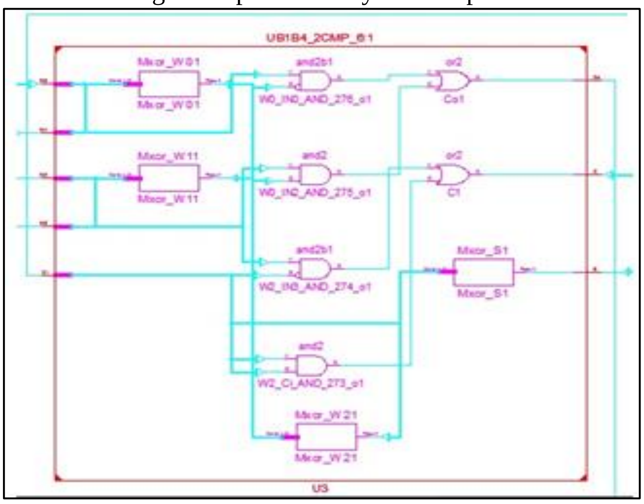

Fig. 5: RTL structure of 4:2 compressors

V. SIMULATION AND RESULTS

Design of high performance compressor based urdhwa-tiryakbhyam multiplier is seen to efficient speed and area in digital design with respect to other multiplier. Considering all the design of it discussed above, we can conclude that the 4:2 Compressor based urdhwa-tiryakbhyam multiplier is best in speed of multiplier. The urdhwa tiryakbhyam multiplier was designed on a xilinx 13.1 Vertex 7 (xc7v285t-3ffg1157) family. Hence the test bench waveform and device utilization summary shown in fig.6 & 7

The delay of high performance compressor based urdhwa-tiryakbhyam multiplier is 8.81nsec.

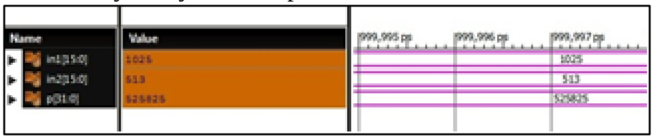

Fig. 6: Result of urdhwa-tiryakbhyam multiplier

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	574	178800	0%
Number of fully used LUT-FF pairs	0	574	0%
Number of bonded IOBs	64	600	10%

Fig. 7: Summary of urdhawa tiryakbhyam multiplier

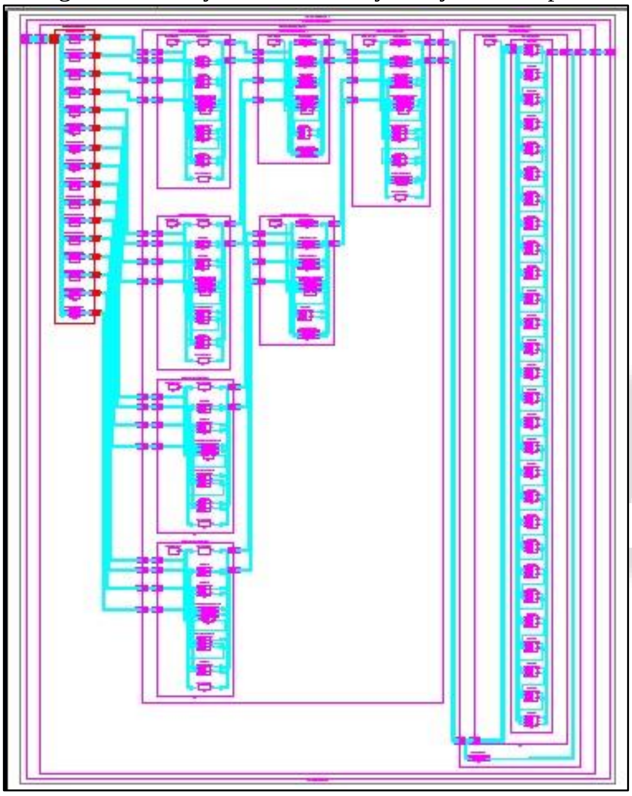

Fig. 8: RTL view of 4:2 compressor based urdhwa-tiryakbhyam multiplier

A. *Comparison of Multiplier*

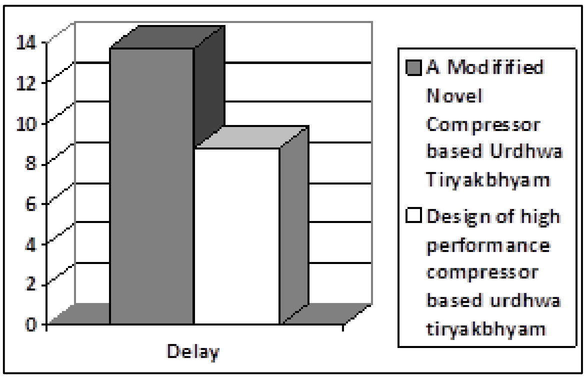

Fig. 9: Comparison Multiplier

Paper	Delay
– A Modified Novel Compressor Based Urdhwa Tiryakbhyam Multiplier.	13.781ns
– Design and Implementation of 16 x 16 Multiplier Using Vedic Mathematics	28.779ns
Praposed Work	**8.81ns**

Table 2: The Paper

The base paper delay is greater so we have to minimise the delay. [1] Shows 8x8 input and 16-bit Output using 4:2 Compressor using vedic mathmatics.

[11] shows 16x16 input and 32-bit output multiplier using vedic mathmatics. Here the delay is 28.779ns.

We also designed multiplier using 4:2 compressors and vedic mathmatics and the delay is reduced to 8.81ns which is less as compared to based paper.

VI. Conclusion

Design of 16 – bit High Performance Compressor Based urdhwa tiryakbhyam Multiplier is proposed. Our design uses 4:2 compressor and replaced several half and full adders required in the circuit. Proposed high performance compressor based urdhawa tiryakbhyam multiplier was developed and compared with existing modified compressor based urdhwa tiryakbhyam multipliers and finally, it is concluded that speed of proposed multiplier is better than existing multipliers. This multiplier is designed on Xilinx 13.1 Vertex 7 (xc7v285t-3ffg1157) family.

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