A Verilog Prototype for Scalable Binary Detector

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Abstract— In this paper a prototype was developed in regard of verilog for overall binary demodulator by considering input chips as the feeder. The prototype developed looks for a prescribed format of chipping signal. When the desired sequence of chip is found the prototype is locked by releasing first output. The algorithm and coding pertaining to this is done and simulated through ModelSim Simulator and is implemented on Xilinx Virtex FPGA device.

Key words: FPGA, Xilinx, ModelSim

I. INTRODUCTION

The digital data which can be commonly seen in computers is mainlty through digital data transfer.

The characteristics that was frustrating is most of information looks alike.It is of prime importance for a receiver to identify the data correctly instead of ambiguity. When a receiver can identify the sequence correctly about the start and end bits of the frame. The typical bit sequence will consider Slag as an efficient mechanism to do this task. The concept of Slag is a bit sequence which helps to identify the stream of bits. To recognize a bit in a bit stream sequence detector is used.

The present paper deals with a universal detector sequence. The prototype was implemented by Verilog HDL. Modelsim was used for simulation and validation test was done on Virtex FPTA prototype model.

A. Field Programmable Gate Array:

For reconfigurable hardware implementations for implementing high digital functions prototype such as FPGA is considered. The high speed efficiency of FPGA through fixed point, parallel computational structures is nearly 100 times when considered to DSP, digital signal processor. The extreme features of FPGA even high complex algorithms to be computed with in less span of time even FPGA are economical.

Virtex prototype developed in FPGA's are ideal for low-cost, highly used applications and are suggested as replacements for fixed-logic gate arrays. The Virtex 4 FPGA along with low cost in budget it also combines many architectural features associated high rated engineering aspects in logic design. The combination of economical cost and variety of efficient usage features has made a better alternative for ASICs (Application Specific Integrated Circuits).

B. Modelsim Simulator:

This simulator used is a Mentor Graphics product which has the capability to simulate integrated programs in Hardware Description Languages. Here the combination of single kernel simulator (SKS) technology with an unified debug environment for Verilog, VHDL, and System C. The combination of industry-leading, native SKS performance with the best integrated debug and analysis environment make ModelSim the simulator of choice for both ASIC and FPGA designs.

II. SYSTEM IMPLEMENTATION

Binary sequences are inserted at the beginning (or end) of the data frame or sub frame emanating from a digital data processor of a space craft. Sequence detectors are used in the detecting equipment on the ground to provide flags which indicate the beginning (or end) of a data block. The sequence detector is in essence an electronic combination lock which is opened for one digit period only when the proper sequence of binary digits is entered. In general sequence detectors can be designed using the state machines. Those detectors which were designed using state machines are limited to detect a particular sequence. As the state machine varies from one required sequence to other, it will be difficult to design a universal detector which will able to detect any sequence of any length.

Universal Scalable Sequence detector design can be achieved if we use a scalable shift register. So we have designed Detector using scalable shift register, which stores the input sequence and compares it with the required sequence to be detected. Scalable register in the sense that, the register facilitates us in storing any number of bits. In general, the required sequence that should be detected is stored in internal register.

Whenever the input binary sequence is applied to the shift register, it takes the sequence bit by bit for every clock cycle and shifts to the right in the next clock cycle. If the sequence resting in the shift register matches with the required sequence, present in the internal register, an output pulse will be generated, acknowledging the user about the detection of the sequence.

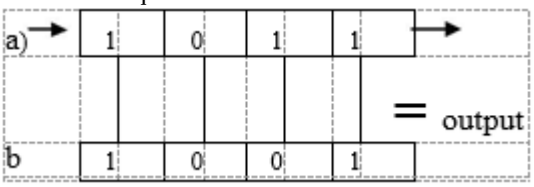

Fig. 1: Representation of Detection of Required Sequence

The representation of detection of required sequence is shown in the above figure. The first block a) containing four memory spaces is the scalable shift register and the second block b) containing four memory spaces represent an internal register. Here in this case the sequence to be detected is 1001, which will be stored in internal register. The Scalable register takes the size of internal register. The major sequence from which the require sequence is to be detected will be carried from the LSB of the shift register to the MSB of it. Whenever the binary contents of the shift register matches with that in the Internal register, an output pulse will be generated. Similarly we can be able to detect any sequence of any length. The sequence to be detected will be stored in the Internal register, shift register of same memory will be generated and then compared, finally detecting the required sequence.

III. SIMULATION RESULTS

The design is simulated in ModelSim PE student Edition Figure 3 shows the timing waveform of the design obtained with ModelSim PE student Edition Simulator for a 8 bit sequence. Design is implemented on Xilinx Virtex 4 XC4VFX12 FPGA device. The top level of RTL schematic obtained by synthesizing the design in Xilinx is shown in Figure 2 and the pins are described in Table 1.

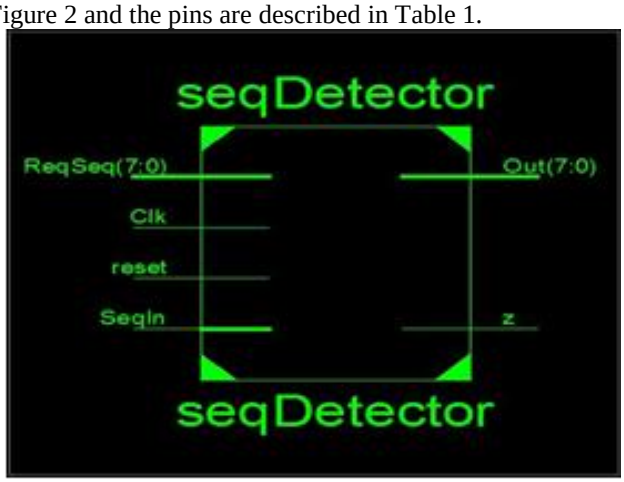

Fig. 2: Top level block diagram of universal Scalable binary sequence detector

Input Signal	Description
ReqSeq(7:0)	Required Sequence to be detected
	here in this example it is of 8 bit
Clk	System Clock signal input
reset	Reset signal input
Seqin	Input binary sequence from which
	required sequence to be detected
Output signal	Description
Out(7:0)	Shift register output at every clock
z	The Output if sequence is detected

Table 1: Pin Description

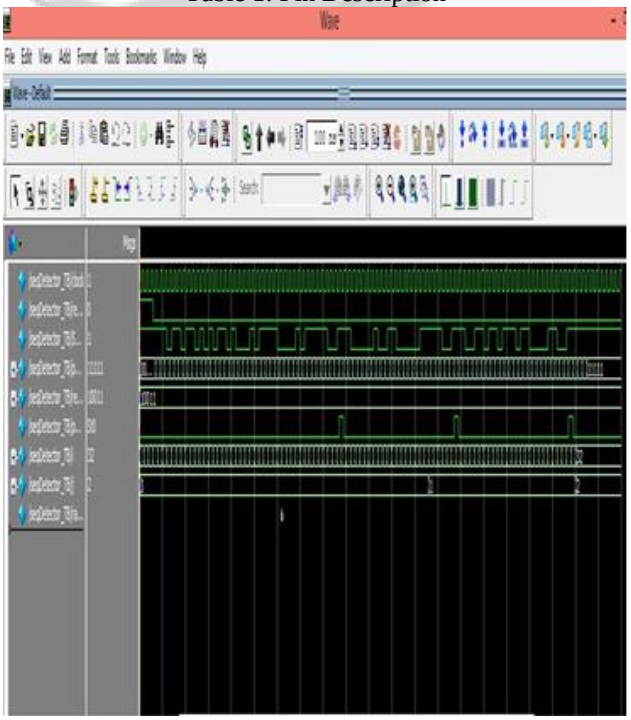

Fig. 3: Simulation results obtained from Modelsim simulator

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	41	10,944	1%
Number of 4 input LUTs	62	10,944	1%
Number of occupied Slices	52	5,472	1%
Number of Slices containing only related logic	52	52	100%
Number of Slices containing unrelated logic	0	52	0%
Total Number of 4 input LUTs	93	10,944	1%
Number used as logic	62		
Number used as a route-thru	31		
Number of bonded IOBs	20	320	6%
IOB Flip Flops	1		
Number of BUFG/BUFGCTRLs	1	32	3%
Number used as BUFGs	1		
Average Fanout of Non-Clock Nets	2.46		

Fig. 4: Device utilization summary

The complete schematic of the design showing all the inputs and outputs at the inside level is shown in Figure 5. In this example it detects the binary sequence of 8 bits. It includes AND gates, Magnitude comparators, D flipflops , NOT gates.

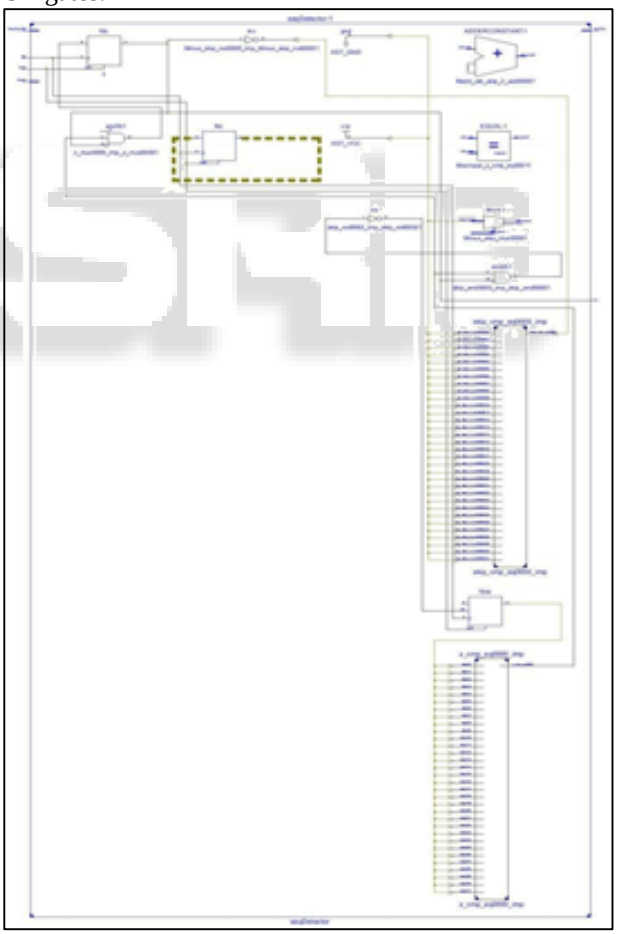

Fig. 5: Internal View Block Diagram of Universal Scalable Binary Sequence Detector

IV. CONCLUSION

In the proposed methodology we have developed a binary universal scalable sequence detector. The methodology implemented in Verilog HDL Hardware Description Language. The mentioned technique was simulated using

ModelSim simulator and was tested for the real time application of the design on Virtex 4 XC FPGA module and the design is analyzed to be efficient. As prototype name suggests it is scalable and can be implemented for the detection of the sequence of any no. of bits within the capacity storage of register.

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