# A Low Power Dynamic Latched Double Tail Comparator: A Review

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*Abstract*— This paper presents a review on the low power dynamic latched double tail comparator designed on Tanner EDA. A new dynamic latched comparator which shows lower power consumption and high speed than the conventional dynamic latched comparators can be designed as per the rising demand of low power and high performance circuits in VLSI.

***Key words:*** ADC, Comparator, Low Power Design, Kick Back Noise

## I. INTRODUCTION

Comparison is a frequently used operation in different logic and arithmetic applications. It is also required in thresholding functions and cells like sense amplifiers. The basic function of a comparator is to compare an analog signal with another analog signal or reference and output a binary signal based on comparison. Since it is easier to distribute voltages to a large number of comparators than to distribute currents, most converters employ voltage comparison. A voltage comparator can be simply regarded as a 1-bit ADC.

In this work we will be conducting a study of different comparator topologies with their merits/demerits and applications. The simulation of a comparator will also be carried out with the help of SPICE to analyze the circuits and calculate the performance parameters like delay, input range, power consumption etc.

A comparator is a device that compares two voltages or currents and outputs a digital signal indicating which is larger. Comparator is a circuit that compares one analog signal with another analog signal or a reference voltage and outputs a binary signal based on the comparison and works on two phases: reset and regeneration phase [1]. It is a very crucial component of an analog to digital converter (ADC).Analog to digital converter is a device that converts a continuous physical quantity (usually voltage) to a digital number. The conversion involves quantization of input, so it necessarily introduces a small amount of error. It is an iterative method. The inverse operation is performed by a digital to analog converter (DAC).

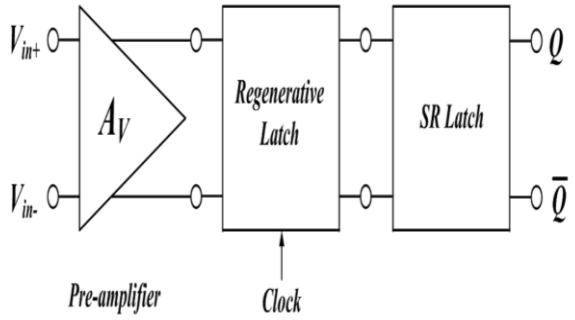


Fig. 1: Typical block diagram of a high-speed voltage comparator

A comparator was defined above as a circuit that has a binary output whose value is based on a comparison of two analog inputs. The output of the comparator is high when the difference between the non-inverting and inverting inputs is positive, and low when this difference. The accuracy of such comparators, which is defined by its offset, along with power consumption, speed is of keen interest in achieving overall higher performance of ADCs. In Fig.1 block diagram has been shown of the conventional three stage comparators in which the first stage is denoted as the main preamplifier, the second stage is a simple gain stage which is also considered as isolating block between preamplifier and latch, and the final stage is attached to output latch [2]. Cascading three blocks requires larger area and power consumption.

## II. LITERATURE REVIEW

Dynamic comparators are being used in today's A/D converters extensively because these comparators are high speed, consume lesser power dissipation, having zero static power consumption and provide full-swing digital level output voltage in shorter time duration. Back-to-back inverters in these dynamic comparators provide positive feedback mechanism which converts a smaller voltage difference in full scale digital level output. However, an input-referred latch offset, resulting from the device mismatches such as threshold voltage, current factor β (=μ.CoxW/L) and parasitic node capacitance and output load capacitance mismatches, limits the accuracy of such comparators [3].

Chandrahash Patel et.al, June 2014 [1] described that a comparator is a device that compares two voltages or currents and outputs a digital signal indicating which is larger. Comparator is a circuit that compares one analog signal with another analog signal or a reference voltage and outputs a binary signal based on the comparison and works on two phases: reset and regeneration phase.

Sarang Kazeminia et. al, 2010 [2] stated that in conventional three stage comparators in which the first stage is denoted as the main preamplifier, the second stage is a simple gain stage which is also considered as isolating block between preamplifier and latch, and the final stage is attached to output latch. Cascading three blocks requires larger area and power consumption.

Sweta sahu et. al, 2012 [3] proposed that dynamic comparators are being used in today's A/D converters extensively because these comparators are high speed, consume lesser power dissipation, having zero static power consumption and provide full-swing digital level output voltage in shorter time duration. Back-to-back inverters in these dynamic comparators provide positive feedback mechanism which converts a smaller voltage difference in full scale digital level output. However, an input-referred latch offset, resulting from the device mismatches such as threshold voltage, current factor β (=μ.CoxW/L) and parasitic node capacitance and output load capacitance mismatches, limits the accuracy of such comparators.

Raja Mohd . et. al, 2012 [4] concluded that the basic comparison between the comparator waveforms should be functional. If the input of the comparator is greater than the reference voltage, Vref, then the output results will be a "1"

 

and if the input voltage is less than reference voltage then the output voltage of the comparators produces output of "0.".

Table 1 shows the comparison of different comparators designed by different techniques. These comparators have different delay and power consumption. By this table conclusion can be made as if a device has a advantage then it also has disadvantages. In low power comparator power consumption is low because of low supply voltage. Low power comparator also having reduced area so chip size is reduced and power consumption also reduced.

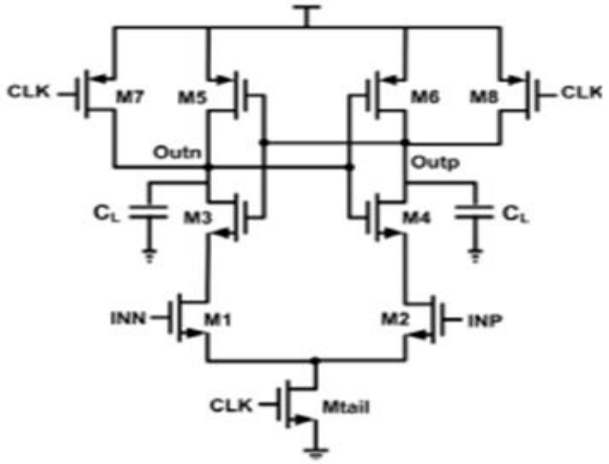


Fig. 2: Schematic of Conventional Comparator

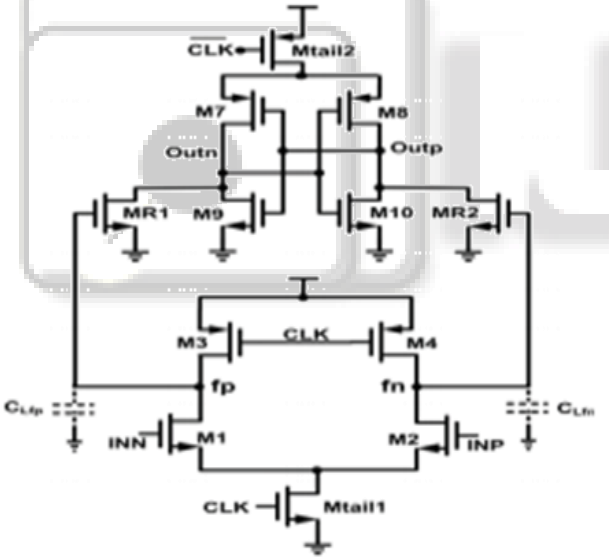


Fig. 3: Schematic of Double Tail Comparator

The schematic diagram of the conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig.3.2 .The operation of the comparator is as follows. During the reset phase when clk = 0 and Mtail is off, reset transistors (M7–M8) pull both output nodes Outn and Outp to VDD to define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK = VDD, transistors M7 and M8 are off, and Mtail is on. Output voltages (Outp, Outn), which had been pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where VINP > VINN, Outp discharges faster than Outn, hence when Outp (discharged by transistor M2 drain current), falls down to VDD–|Vthp| before Outn (discharged by transistor M1 drain current), the corresponding pMOS transistor (M5) will turn on initiating the latch regeneration caused by back-to-back inverters (M3, M5 and M4, M6). Thus, Outn pulls to VDD and Outp discharges to ground. If VINP < VINN, the circuits works vice versa.

The operation of this comparator is as follows (Fig4). During reset phase (CLK = 0, Mtail1, and Mtail2 are off), transistors M3-M4 pre-charge fn and fp nodes to VDD, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground. During decision-making phase (CLK = VDD, Mtail1 and Mtail2 turn on), M3-M4 turn off and voltages at nodes fn and fp start to drop with the rate defined by IMtail1/C fn(p) and on top of this, an input-dependent differential voltage Vfn(p) will build up. The intermediate stage formed by MR1 and MR2 passes Vfn(p) to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise .After the first n-channel transistor of the latch turns on (for instance, M9), the corresponding output (e.g., Outn) will be discharged to the ground, leading front p-channel transistor (e.g., M8) to turn on, charging another output (Outp) to the supply voltage (VDD). In this comparator, both intermediate stage transistors will be finally cut-off, (since fn and fp nodes both discharge to the ground), hence they do not play any role in improving the effective trans conductance of the latch. Besides, during reset phase, these nodes have to be charged from ground to VDD, which means power consumption. An offset cancellation technique can be used to implement a high speed analog to digital converter such as Flash ADCs. An offset cancellation network is placed in the structure of comparator, it increases the transistor count. Supply boosting technique is very suitable for very low power clocked and continuous time circuits. In UDSM technology area is reduced but performance degrades. Latch is modified by stacking of transistors. There always some tradeoffs in a design as if supply voltage is reduced the overall performance degrades but for low power consumption it is necessary. To ensure correct detection on each comparison, the analog input must have sufficient magnitude to overcome deterministic errors such as offset and hysteresis, as well as random errors due to device thermal noise and flicker noise. In present time everything has to be operated with less power consumption. Delay also a function of power consumption. In low power comparator power consumption is low because of low supply voltage. Low power comparator also having reduced area so chip size is reduced and power consumption also reduced. This structure has the advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch. Due to the fact that parasitic capacitances of input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset.

Important drawback of this structure is that there is only one current path, via tail transistor Mtail, which defines the current for both the differential amplifier and the latch (the cross-coupled inverters). While one would like a small tail current to keep the differential pair in weak inversion and obtain a long integration interval and a better Gm/I ratio, a large tail current would be desirable to enable fast regeneration in the latch, Besides, as far as Mtail operates

 

mostly in triode region, the tail current depends on input common-mode voltage, which is not favorable for regeneration. In many well supplied devices the problem related to power is essentially related to cost. However for the low-powered devices the problem of power is not only economics but also becomes very essential in terms of functionality. Due to the usual very small amount of energy or unstable energy available the way the engineer manages power becomes a key point in this area. In present time everything has to be operated with less power consumption.

## III. CONCLUSION

It is known that comparator is mainly used in ADCs and relaxation oscillators. But it should be low power consummator during active operation and in sub-threshold condition. A comparator consists of a specialized high-gain differential amplifier. They are commonly used in devices that measure and digitize analog signals, such as analog-to-digital converters. By only strobing a comparator at certain intervals, higher accuracy and lower power can be achieved with a clocked (or dynamic) comparator structure.

## IV. FUTURE SCOPE

As mentioned earlier, since the proposed fully dynamic latched comparator can be optimized for either the minimum kickback noise voltage or the maximum load drivability at a limited area according to the design specification, searching for the most suitable application can be one topic for the future works. In addition, kickback noise cancellation techniques can be considered for further reduction of the kickback noise voltage.

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