Designing and FFT Analysis of Sigma Delta Converter using Spice

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Abstract— This paper explains the function of a Sigma Delta analog-to-digital converter. The first-order 1-Bit Sigma-Delta (Σ-Δ) modulator is designed and simulated using LTspice standard 180nm CMOS technology power supply of 2.5V. The modulator is proved to be robustness, the high performance in stability. Here a sinc filter is an additional component by which a 5 bit sinc filter 2nd order sigma delta is design. The FFT analysis of modulator, integrator and the sigma delta converter is also calculated here. The designed has gain of 52.788db, phase margin of 59.44 deg, power consumption of 61.49µW at a power supply of SINE (2.5 2.5 50k).

Key words: FFT, Sigma Delta Converter

I. INTRODUCTION

A Sigma Delta modulator is the most striking feature of a sigma delta ADC, it is the main component of sigma delta ADCs, because these modulators use a very high sampling rate. The sampling rate used is in the range of MHz, which is much higher than the Nyquist rate, normally in the range of kHz. Hence, the oversampling ratio is very high, because of which these are sometimes referred to as oversampling ADCs. The advantage of using this very high sampling ratio is high resolution of the digital output and better noise shaping. Sigma-Delta modulation depend on analog to digital conversion methodology is an effective alternative for high resolution converters. This type of technique is not only cost efficient but also can be integrated on DSP Ics. Increased use of digital technology in communication field propelled the introduction of cost effective high resolution A/D converters.

The main components of a sigma delta modulator are: a summer, an integrator, a comparator and a DAC. The difference of the analog input and the output of the modulator, feedback to the input through a DAC, and it is fed to the integrator. The integrator ramps up or down depending upon whether the difference being fed is positive or negative. The output of the integrator goes into a comparator. The comparator produces 5V or 0V depends on whether the output of the integrator is above or below the threshold voltage being compared by the comparator. The comparator's output is fed in to a DAC. The output of this DAC is fed to the summer at the input stage. Sigma Delta ADC design contain the components Operational amplifier as an integrator, Comparator at the place of quantizer and we replace the feedback 1-bit DAC by a behavioral Schmitt-triggered inverter with differential input.

- Op-amp (active integrator)
- Comparator (Quantizer)
- 1-Bit DAC (Inverter)

II. SIGMA DELTA DESCRIPTION

This ADC known by various names such as Sigma-Delta ADC, Delta Sigma ADC, Over-sampling ADC, noise shaping ADC, 1-bit Delta-Sigma ADC. Name comes from the architecture of the modulator which integrates (Sigma) the difference (Delta) between the input and the quantized output. Sigma Delta modulator is the basic design of Sigma Delta ADC. The basic design consist ideal comparator as a quantizer and inverter in a feedback loop replacing the 1-bit DAC

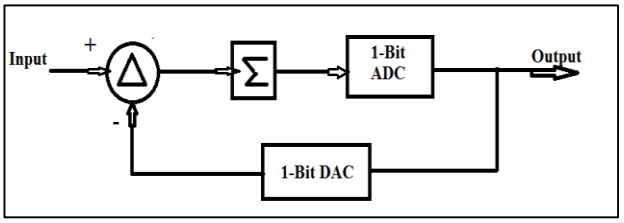

Fig. 1: Sigma Delta Modulator

The resistors R1 and R2 convert voltage in to current, it shows linear relationship due to Ohm's Law(V=IR). Currents summed to form difference (feedback is inverted), capacitor provides integration. Comparator used as 1-bit ADC and inverter used as 1-bit DAC. This work as a simple modulator shown in Fig.2.

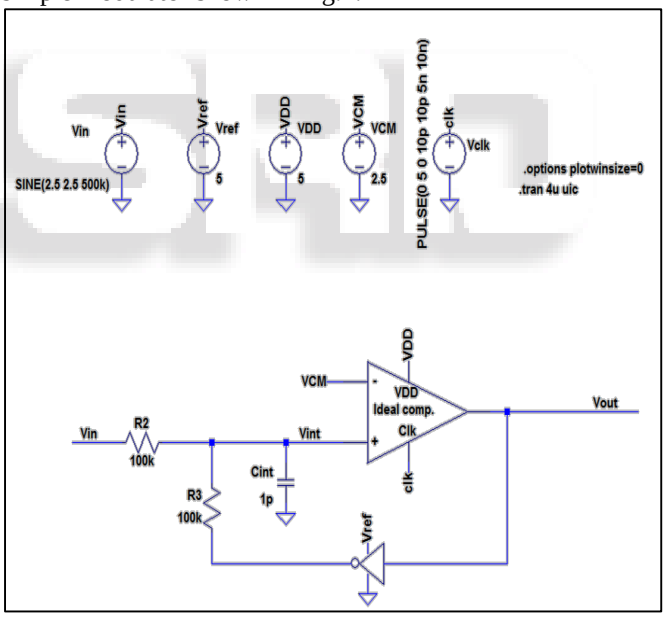

Fig. 2: Schematic Simple Modulator

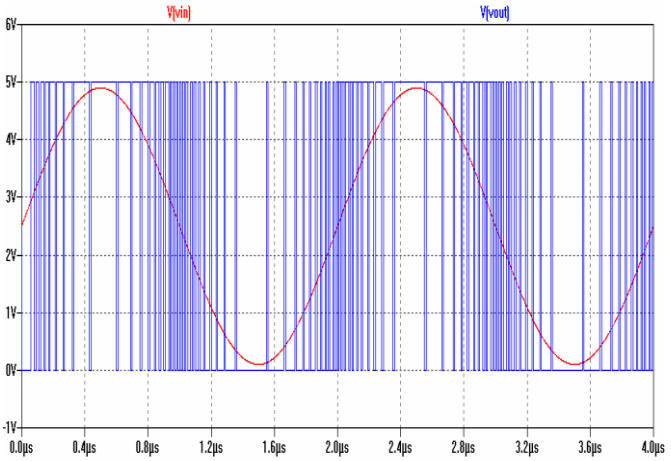

Fig. 3: Simple Modulator Output

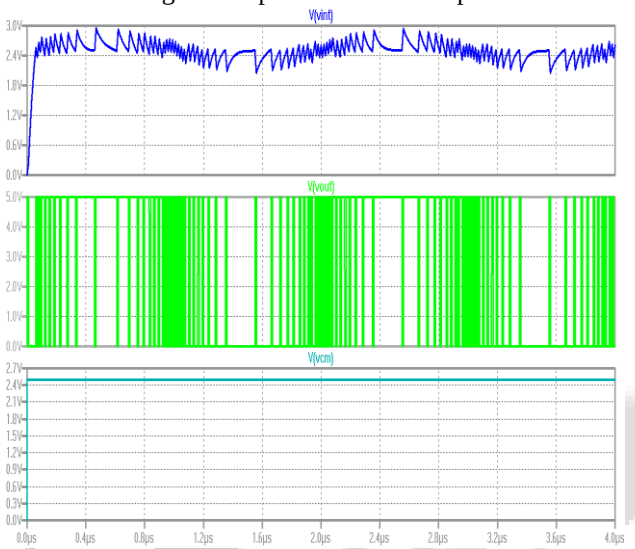

Fig. 4: Variation in V(vint), V(vout) and V(vcm)

Feedback tries to hold the voltage across the capacitor at Vcm. For the voltage across the capacitor to remain constant, there must be zero net current into the capacitor. For there to be zero net current into the capacitor, the feedback current must be equal and opposite to the input current The feedback voltage (converted to a current) can only take on one of two levels, it cannot exactly match –Vin The duty cycle of the feedback is varied so the average voltage (current) feedback is equal and opposite to the input.

If we use a counter on the output, we can measure the duty cycle of the feedback which is equal to the input. If we measure for a longer period of time, we get more accuracy.

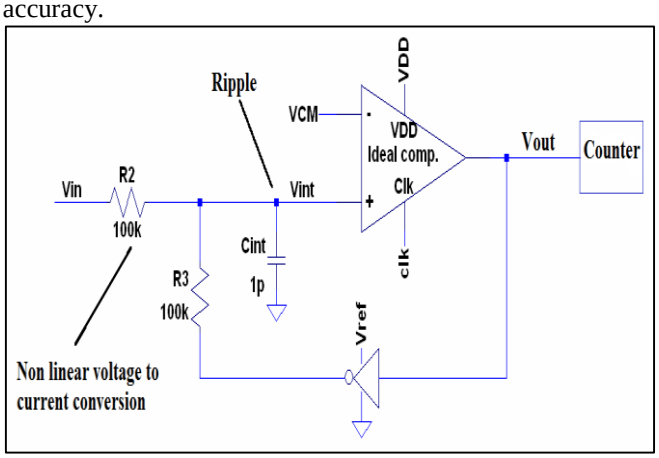

Fig. 5: Error caused by modulator Ripple

Ripple on Vint causes non-linear voltage to current conversion resulting in distortion and limiting achievable accuracy.

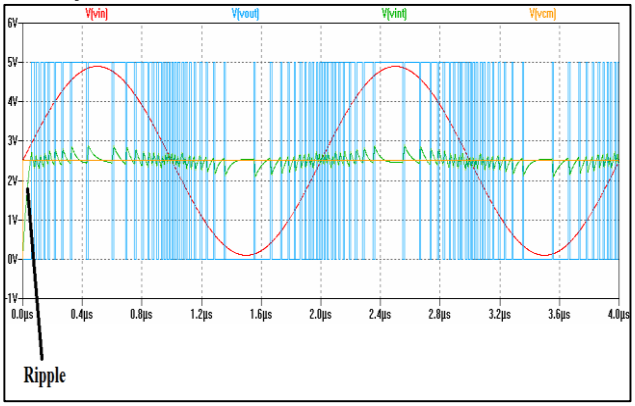

Fig. 6: Output showing error caused by modulator ripple

III. DESIGN OF OPERATIONAL AMPLIFIER

In this paper we are eliminating ripple on sigma delta ADC by using an active integrator to hold input voltage constant Charge transferred to integration capacitor is the difference in input current minus the feedback current integrated over one clock period

$$Q = (I_{in} - I_{fb}) * t = \frac{(V_{in} - V_{out})}{R^*}$$

The active integrator is work as similar to an ideal Op-amp which is in fig.7

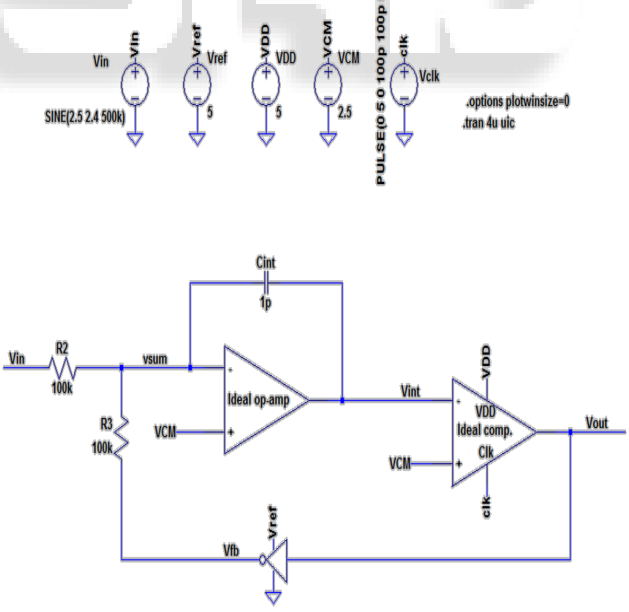

Fig. 7: Schematic of Active Integrator

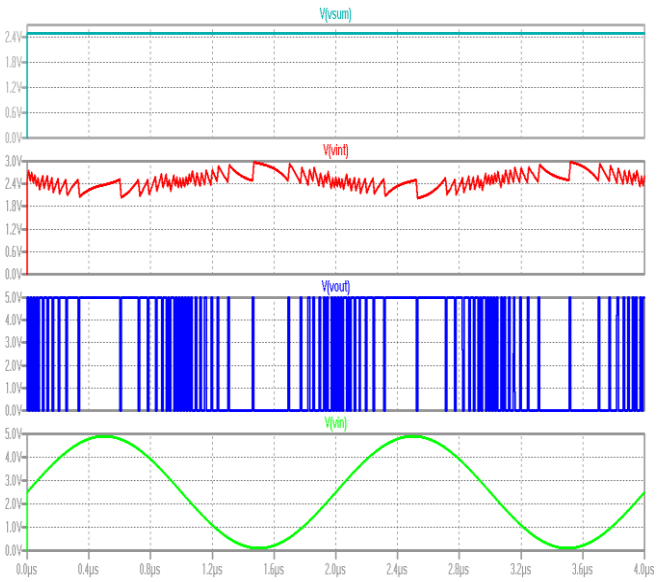

Fig. 8: Output of an Active Integrator

The above fig.8 shows the variation of V(vint), V(vout) and V(vsum) with the variation of input voltage that is V(vin),

IV. DESIGN OF COMPARATOR

A comparator work as the quantizer in the first order modulator. Since the comparator is of 1-Bit it has only two levels either a 1 or a 0. If the integrator output is greater than the reference voltage (Vref) it has to give an output of "1", and if the output of the integrator is less than reference voltage then the output of the comparator should be "0". A simple comparator performs the necessary function efficiently. The operational amplifier can be used as a comparator. The only change required is that the comparator does not need the compensation network because its only function that is to switch from rail to rail. Stability is not required as it will only slow down the switching speed. Whenever a sine wave is input to the circuit, the comparator switches from positive rail to negative rail.

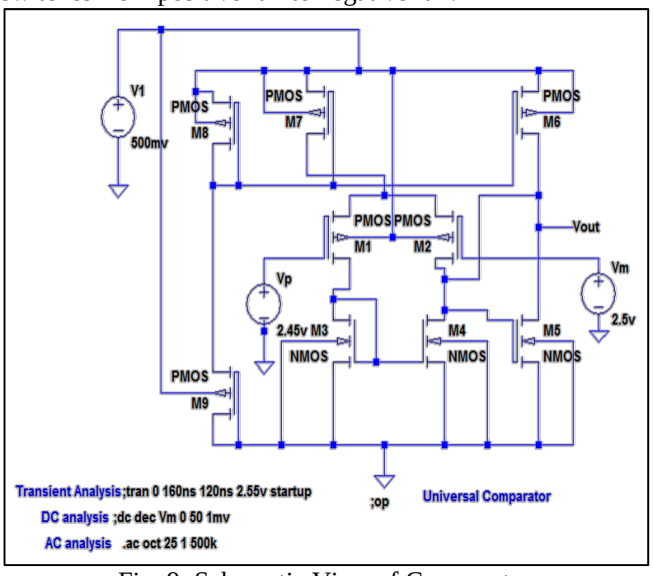

Fig. 9: Schematic View of Comparator

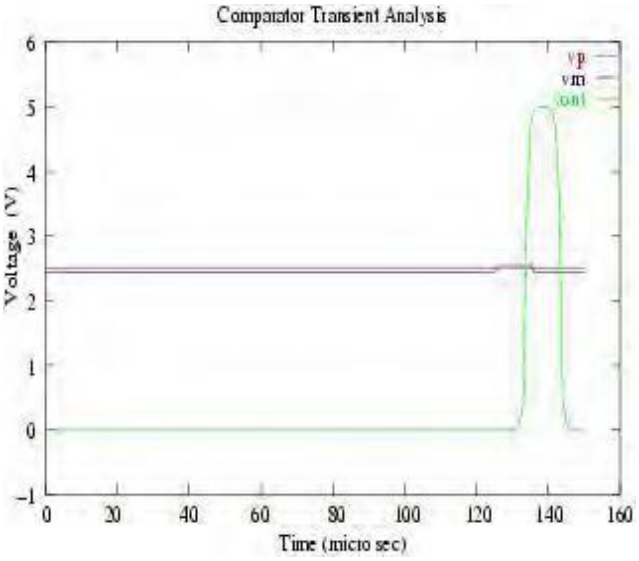

Fig. 10: Transient Response of Comparator

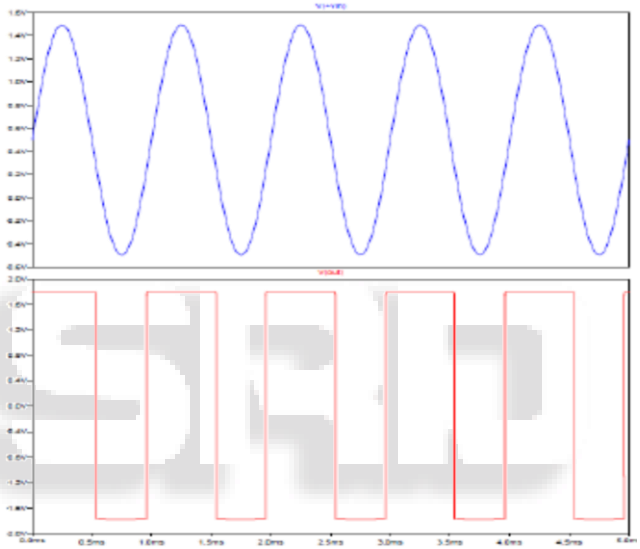

Fig. 11: Output of Comparator

V. DESIGN OF 1-BIT DAC

The most popular digital-to-analog converter application is converting stored digital audio and/or video signals. For example, stored digital information in MP3 format can be converted into music via a high-precision DAC

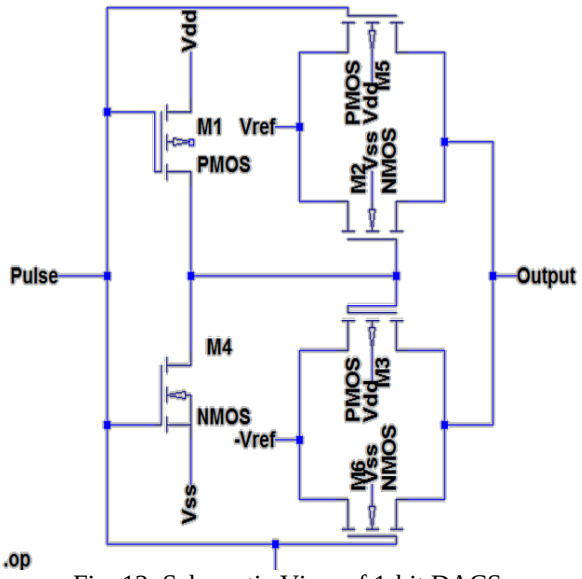

Fig. 12: Schematic View of 1-bit DACS

VI. SIGMA DELTA CONVERTER USING SINC FUNCTION

A sinc filter is an additional component by which a 2nd order 5 bit sinc filter sigma delta converter is design. Here the value of Vdd is 5v,Vref is also 5v. Two clocks are providing first clock is PULSE(0v 5v 10n 0.1n 0.1n 4n 10n) and the other clock is PULSE(0v 5v 5n 0.1n 0.1n 4n 10n). An additional Voltage reset that is Vrst is PULSE(5v 0v 25n 0.1n 0.1n 10m). The transient analysis is perform at the 25u is the stop time.

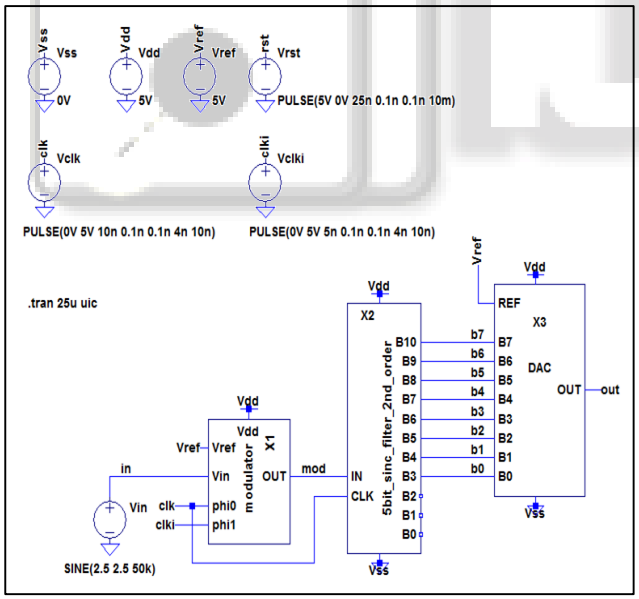

Fig.13: Schematic of Sigma Delta Converter

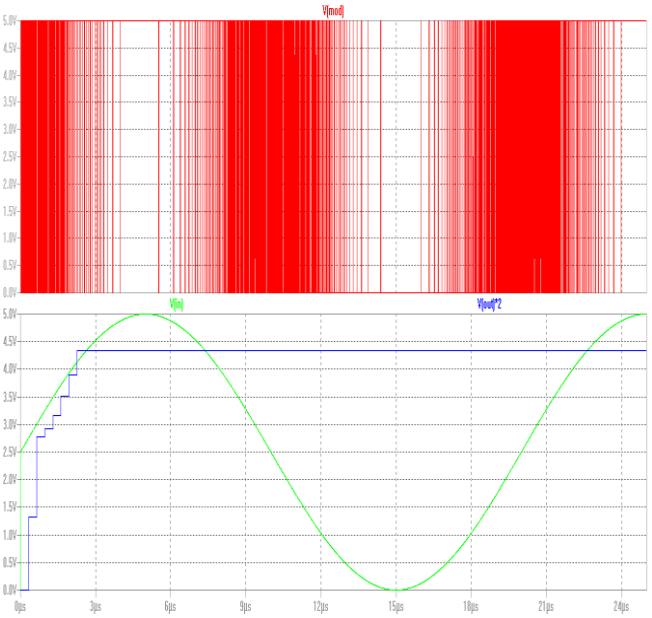

Fig. 14: Output of Sigma Delta Converter

VII. FFT ANALYSIS AND SIMULATION RESULTS

The design and experimental results of a Simple modulator, active integrator and sigma delta converter has been presented.

The FFT analysis of modulator, integrator and the sigma delta converter is also calculated here. The designed has gain of 52.788db, phase margin of 59.44 deg, power consumption of 61.49µW at a power supply of SINE(2.5 2.5 50k).

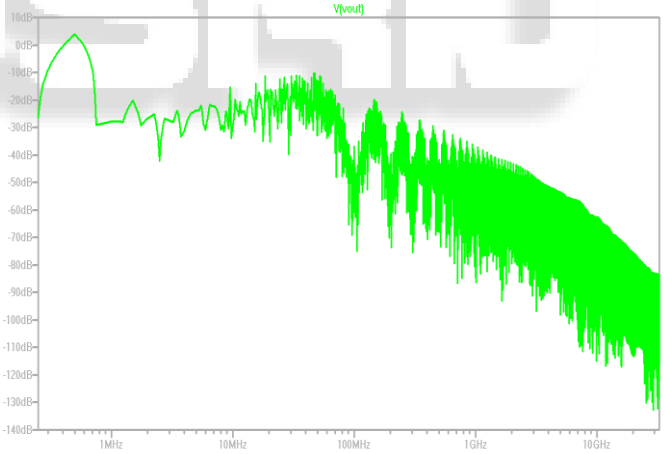

Fig. 15: FFT for Simple Modulator

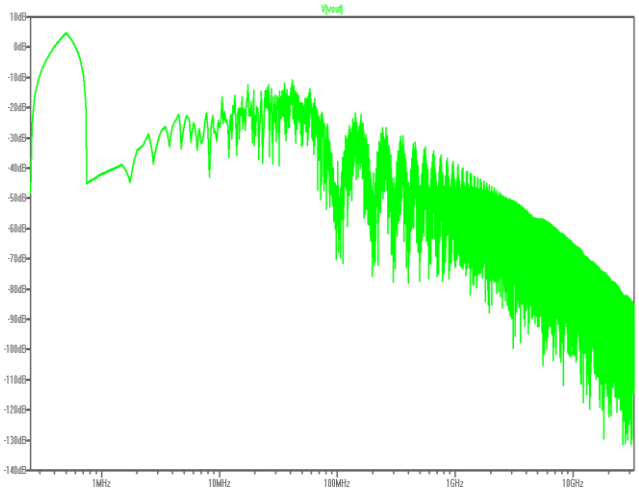

Fig. 16: FFT for Active Integrator

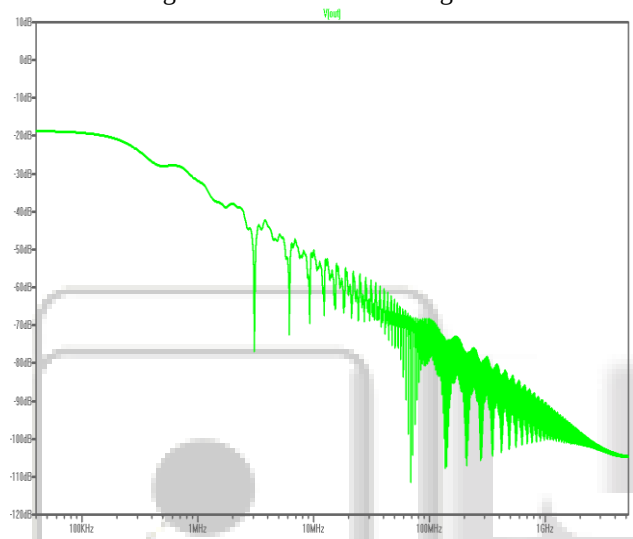

Fig. 17: FFT of 2nd order Sigma Delta Convert

VIII. RESULTS THROUGH TABLES

Frequency	Magnitude(db)	Phase(*)	Group Delay(ns)
1Mhz	-27.8338	167.864	73.231
10Mhz	-28.8827	96.414	249.093
100Mhz	-40.445	-107.658	-405.695
1Ghz	-60.251	105.379	365.214
2Ghz	-64.199	-132.939	-352.989
5Ghz	-67.660	13.813	439.787
8Ghz	-86.652	134.704	861.642
10Ghz	-76.738	139.674	563.648

Table 1: FFT Analysis of Simple Modulator

Frequency	Magnitue (db)	Phase(*)	Group Delay(ns)
1Mhz	-41.846	-82.383	-570.132
10Mhz	-26.33	34.15	768.01
100Mhz	-40	-188.4	-490.183
1Ghz	-59.66	89.185	228.77
5Ghz	-60.319	2.176	-237.62
10Ghz	-73.97	62.43	693.84

Table 2: FFT Analysis of Integrator

Frequency	Magnite (db)	Phase(*)	Group Delay(ns)
1Khz	-19.22	154.7	676.715
1Mhz	-31.934	91.702	90.988
10Mhz	-50.585	89.642	245.934
100Mhz	-76.719	76.688	-100.828
1Ghz	-93.090	88.245	-64.208
5Ghz	-104.622	174.811	-1.161

Table 3: FFT Analysis of Sigma Delta Converter

IX. CONCLUSION

The LTspice IV 4.21b, SPICE simulations using SPICE level-1 MOS model parameters. The circuit design of Op-amp, Comparator and DAC for first order Sigma- Delta (Σ-Δ ADC) have been developed and implemented by using 180nm CMOS Technology proposed 2nd order sinc filter can achieve a maximum gain of 52.788db, power consumption of 61.49µW at a input supply of voltage is SINE (2.5 2.5 50k).

REFERENCES

[1] Prince Kumar Pandey, "Design and Simulation of First Order Sigma-Delta Modulator Using LT spice Tool," International. Journal of Engineering Research and Applications, ISSN : 2248-9622, Vol. 4, Issue 7 (Version 3), July 2014, pp.16-19.

[2] Jamuna G and Siva S Yellampalli ,"Design and Analysis of CMOS Telescopic OTA for 180nm Technology," International Journal of Engineering Sciences Paradigms and Researches (IJESPR) (Vol. 15, Issue 01) and (Publishing Month: July 2014).

[3] Simranpreet kaur, Dr. Charanjit Singh, "Sigma Delta Converters," International Journal of Engineering Science and Innovative Technology (IJESIT) Volume 2, Issue 5, September 2013.

[4] Arpit R. Patel ,"Performance Analysis of Sigma Delta ADC Using 45nm CMOS Technology," International Journal for Scientific Research & Development| Vol. 2, Issue 01, 2014.

[5] R. Jacob Baker (2009). CMOS Mixed-Signal Circuit Design (2ndEd.).Wiley-IEEE.ISBN978-0-470-29026.

[6] The Design of Sigma Delta Modulation ADC Converters" IEEE Bernhard E Boser student member IEEE , IEEE JOURNAL OF SOLID-STATE CIRCUITS. 7, 1988.

[7] Tong Ziquan, Yang Shaojun, Jiang Yueming and Dou Naiying, "The Design of a Multi-bit Quantization Sigma-delta Modulator", International Journal of Signal Processing, Image Processing and Pattern Recognition Vol.6, No.5 (2013), pp.265-274.

[8] W. Singor & W. M. Snelgrove, "Switched-Capacitor Bandpass Delta-Sigma A/D Modulation at 10.7 MHz", IEEE J. of Solid-State Circuits, vol. 30, no. 3, pp.184-192, March 1995.

[9] S. Bazarjani & M. Snelgrove, "A 40 MHz IF Fourth-order Double-Sampled SC Bandpass Sigma-Delta Modulator", Proceedings of IEEE International Symp. on Circuits & Systems, June 1997.

[10] Kalpesh B. Pandya, Kehul A. shah "Design and analysis of CMOS telescopic operational transconductance amplifier for 0.35µm technology" international journal of science and research, volume 2, issue 3, march 2013.

