Low Cost Design of MOD-8 Synchronous UP/DOWN Counter using Reversible Logic Gate

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Abstract— The Reversible logic synthesis technique is most important part of the long-term future of computing due to its low power dissipating characteristic. Reversible logic gates are very much in demand for the future computing technologies as they are known to produce zero power dissipation under ideal conditions. Today, reversible logic circuits have substantial attention in improving the field of nanotechnology, quantum computing, and low power design of circuits. In this paper we proposed the design of low cost MOD-8 synchronous up/down counter with reduced number of reversible logic gate, constant inputs and garbage outputs using existing reversible gate.

Key words: Reversible logic gate, Counter, Constant input, Garbage output, Delay

I. INTRODUCTION

In [1], Landauer states that the loss of one bit of information dissipates KTln2 joules of energy, where K is the Boltzmann constant and T is the absolute temperature at which the operation is performed. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components. This computation procedure is irreversible. Further Bennett [2], showed that one can avoid KTln2 joules of energy dissipation from the circuit if input can be extracted from output and it would be possible if and only if reversible gates are used. Research is going on in the field of reversible logic and a good amount of research work has been carried out in the area of reversible combinational logic. However, there is not much work in the area of sequential circuit like flip-flops, counters etc. A counter is a sequential circuit capable of counting the number of clock pulses that have arrived at its clock input. This paper proposes the design of low cost MOD-8 synchronous up/down counter with reduced number of reversible logic gate, constant inputs and garbage outputs using existing reversible gates.

II. BASIC CONCEPTS

A. Reversible Logic Function

It is an N×N logic function in which there is a one-to-one correspondence between the inputs and the outputs, N is the number of inputs and outputs. The input vector can be uniquely determined from the output vector. This prevents the loss of information which is the root cause of power dissipation in irreversible logic circuits [3].

B. Garbage Output

A garbage output is an output that is needed to change an irreversible gate to a reversible one and are not used to the input to the other gates [3].

C. Quantum Cost

The quantum cost of a reversible gate is the number of 1x1 and 2x2 reversible gates. The quantum costs of all reversible 1x1 and 2x2 gates are taken as unity. Since every reversible gate is a combination of 1 x 1 or 2 x 2 quantum gate, so the quantum cost of a reversible gate can be calculated by counting the numbers of quantum gate[3][6].

D. Reversible Gate

A gate with equal number of input and output in which input and output have one –to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. If the input vector of a reversible gate is denoted by $I_V= (I_1,I_2,I_3,\ldots,I_K)$, the output vector can be represented as $O_V=(O_1,O_2,O_3,\ldots,O_K)$. A reversible gate can be represented as K×K in which the number of input and output is K [6].

– Reversible NOT gate

The reversible NOT gate is a simplest 1×1 gate [3], Fig. 1 shows the reversible NOT gate with zero quantum cost.

Fig. 1: Diagram of reversible NOT gate

– SVS gate

A SVS gate[4] is a 4 inputs 4 outputs (4×4) reversible gate having the mapping (A, B, C, D) to (P = A, Q = BC'⊕A'B⊕AB'C, R =BC'⊕A'B⊕AB'C⊕D, S=A'C⊕AB), where A, B, C, D are the inputs and P, Q, R, S are the outputs, respectively. Fig. 2 shows the SVS gate.

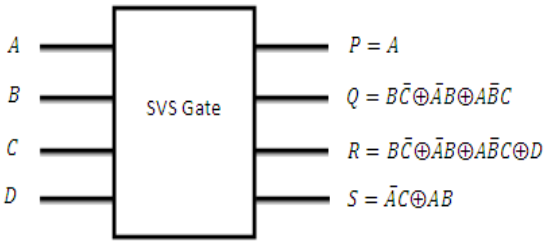

Fig. 2: Block diagram of 4X4 SVS gate.

– SAM Gate

A SAM gate [5] is a 3 inputs 3 outputs (3×3) reversible gate having the mapping (A, B, C) to (P = A', Q = A'B⊕AC', R =A'C⊕AB), where A, B, C are the inputs and P, Q, R are the outputs, respectively. Fig. 3 shows the block diagram of SAM gate and Fig. 4 shows the OR and AND operation of SAM gate.

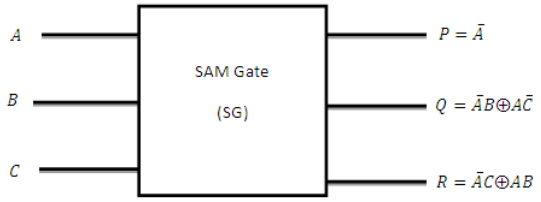

Fig. 3: 3X3 Block diagram of SAM gate

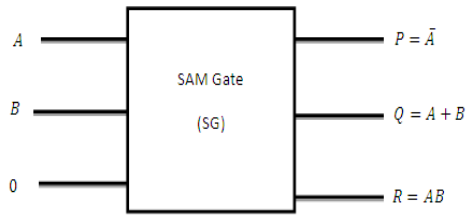

Fig. 4: 3X3 Block diagram of SAM gate

E. Clocked T Flip-Flop

The characteristic equation of a clocked T flip-flop is Q=(T⊕Q).CLK⊕CLK'. The equation can be simplified as Q=(T.CLK)⊕Q. This clocked flip-flop is realized by only one reversible SVS gate [4] shown in Fig. 5.

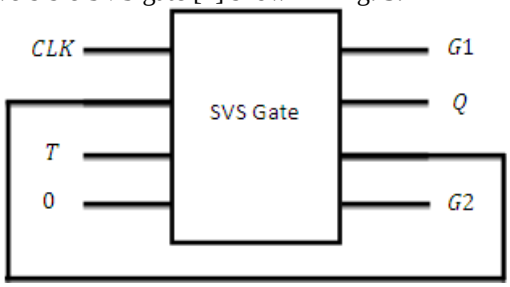

Fig. 5: T Flip-Flop using SVS gate

III. PROPOSED WORK

The Block diagram of 3-bit Up/Down counter is shown in Fig. 6.

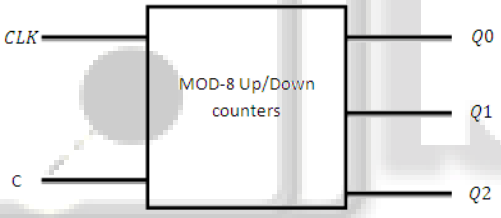

Fig. 6: Block diagram of 3-bit Up/Down counter

From Fig. 6, when C=1, the counter will work in the Up mode, i.e. it counts from state 000 to state 111, when C = 0, it will work in the down mode, i.e. it counts from state 111 to state 000. The table-1 shows the excitation table of proposed work.

Control Input	Present State			Next State			Excitation Inputs		
C	q_2	q_1	q_0	Q_2	Q_1	Q_0	T_2	T_1	T_0
0	0	0	0	1	1	1	1	1	1
0	0	0	1	0	0	0	0	0	1
0	0	1	0	0	0	1	0	1	1
0	0	1	1	0	1	0	0	0	1
0	1	0	0	0	1	1	1	1	1
0	1	0	1	1	0	0	0	0	1
0	1	1	0	1	0	1	0	1	1
0	1	1	1	1	1	0	0	0	1
1	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	1
1	0	1	0	0	1	1	0	0	1
1	0	1	1	1	0	0	1	1	1
1	1	0	0	1	0	1	0	0	1
1	1	0	1	1	1	0	0	1	1
1	1	1	0	1	1	1	0	0	1
1	1	1	1	0	0	0	1	1	1

Table 1: Excitation table for MOD-8 UP/DOWN Counter

Derived Equations excitation table using K-Map for T_2, T_1, T_0 are as follows:

T_2=C'Q1'Q0'+CQ1Q0..... Equation 1

T_1=C'Q0'+CQ0 ……..... Equation 2

T_0=1 ……..... Equation 3

Implementation of these derived equations 1, 2, 3 are shown in our proposed design in Fig. 7 of MOD-8 UP/DOWN Synchronous Counter using reversible gates NOT, SVS gate and SAM gate.

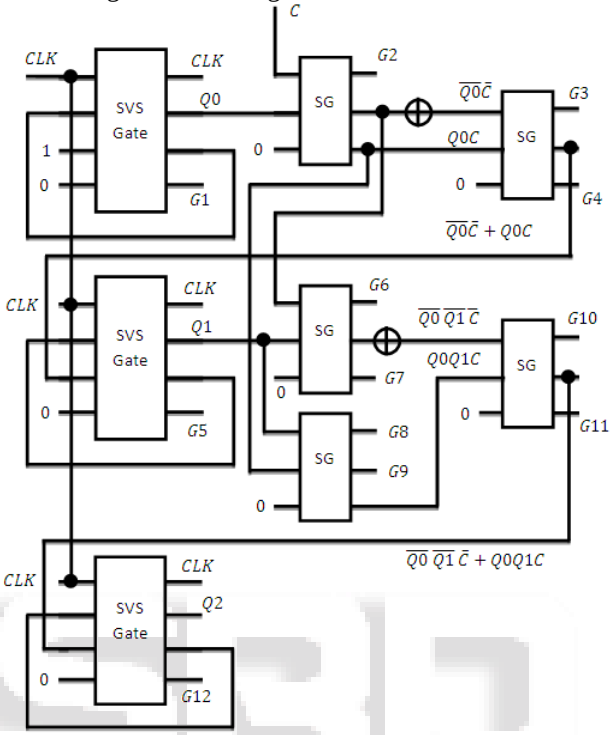

Fig. 7: Proposed Design of MOD-8 UP/DOWN Synchronous counters

IV. RESULTS AND DISCUSSION

In the implementation of MOD-8 UP/DOWN Synchronous counter we use three SVS gate, five SAM gate and two NOT gate, so only ten reversible gate required to design proposed counter. Table-2 shows the comparison results of proposed work.

Parameters	Existing[7]	Existing[8]	Proposed
No. of gates	17	14	10
No. of constant inputs	13	12	9
Garbage outputs	12	12	12

Table 2: Comparison result of MOD-8 Up/Down synchronous counter

V. CONCLUSION

We have presented the basic concepts of reversible gates. This paper proposes improved design MOD-8 reversible synchronous up/down counter which requires less number of reversible gates, garbage output and constant inputs. Here in this paper the proposed designs are better in terms of number of reversible gate and garbage outputs. The proposed synchronous counter designs have the applications in reversible ALU, reversible processor, nanotechnology, low power circuit design etc.

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