

Low Power Full-Adder Design with Gate-Diffusion-Input MUX

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Abstract— This paper proposes a new method for implementing a low-power full-adder-circuit by means of a set of Gate-Diffusion-Input cell based-multiplexers. Full-adder is a very important part of all digital-circuits and it can be used in variety of Application-Specific-Integrated-Circuits (A-S-I-Cs). If the energy usage of a circuit in VLSI chip is very less, it'll be most important aspect for the designer. Here the technique used to realize the FA uses less energy and works faster than conventional one. The simulation readings and outputs using a simulation tool illustrate the outputs that can be compared with the conventional CMOS FA. Energy usage, speed-of-circuit and area-on-silicon, comparison between conventional and proposed full adder is also illustrated.

Key words: Gate-Diffusion-Input MUX, Full-Adder Design

I. INTRODUCTION

The current generation of nanotechnology progressed very fast from the previous technology, resulting in lesser energy requirement and speed of operation will be higher compared to previous generation. Because of the nanotechnology in the electronics, the need for smaller and smarter devices increases gradually these days. Now-a-day, increase in applications in all electronic devices increases complexity of the circuit also, and the operation-speed and portability-of-the-device becoming inevitably major concerns of any smart-device it needs smaller, less-energy consuming & maximum performance circuitry. Hence, circuits of any VLSI- chip are required to work with high-speed and should take low-power. In order to minimize sneak paths, charge sharing, and switching delays of the circuit all the sub-circuit component has to be arranged obeying the VLSI design rules. Ensuring this simulation of circuit schematics provides a platform to verify circuit performance [1]. In order to minimize sneak paths, charge sharing, and switching delays of the circuit all the sub-circuit component has to be arranged obeying the VLSI design rules. Ensuring this simulation of circuit schematics provides a platform to verify circuit performance [2]. To get better speed and power consumption results lot of approaches have been recently proposed [3]-[5]. Among them, two have been established by Hitachi CPL [4] and DPL [4]. In 1993 Hitachi demonstrated a 1.5ns 32-bit ALU in 0.25µm CMOS technology [4] and 4.4ns 54X54 bit multiplier [5] using DPL technique.

II. FULL-ADDER

By considering the full-adder the SUM and CARRY outputs are given as the below functions of the three input variables X, Y and Z.

$$\text{SUM} = (X) \text{ EX-OR } (Y) \text{ EX-OR } (Z)$$

$$\text{CARRY} = (X.Y) \text{ OR } (Y.Z) \text{ OR } (X.Z)$$

These functions can be implemented with CMOS as shown below,

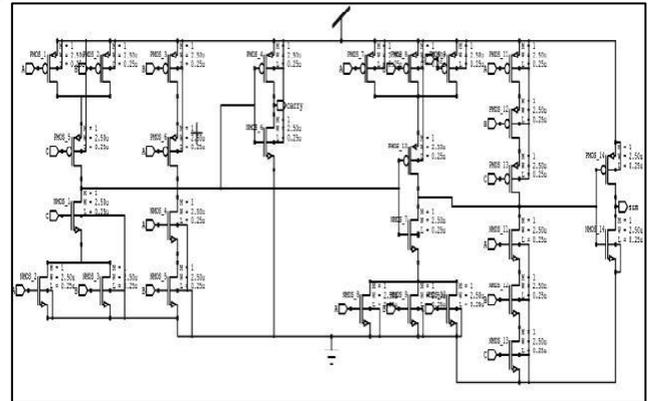


Fig. 1: Full-adder using 28 transistors (conventional CMOS design)

If the Gate-Diffusion-Input technique is used to implement FA, it works much faster and uses less-power compared to other FA designs.

III. GATE-DIFFUSION-INPUT

The Gate-Diffusion-Input cell is shown in Fig. 2. This is arrangement for achieving low power advanced logical circuit. Gate-Diffusion-Input system is essentially 2-transistor usage of complicated rationale works which gives in-circuit voltage-swing reclamation under particular working scenario. This idea prompts lessening in energy utilization, spread postpone and zone of computerized circuits is gotten while having low intricacy of rationale outline. An imperative element of Gate-Diffusion-Input cell is that the wellspring of the PMOS in a Gate-Diffusion-Input cell is not associated with V-D-D and the wellspring of the N-M-O-S is not associated with GND. Consequently Gate-Diffusion-Input circuit gives two additional info sticks for utilize which makes the G-D-I outline more adaptable than CMOS plan. The Gate-Diffusion-Input cell has three input lines, namely, G (shorted gate line of both pmos and nmos device), P (source of the pmos device), N (source of the nmos).

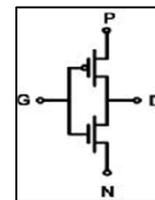


Fig. 2: Gate-Diffusion-Input Circuit

Table-1 depicts diverse rationale works actualized by GDI rationale taking into account distinctive info values. In this way, different rationale capacities can be actualized with less power and rapid with GDI procedure when contrasted with ordinary CMOS plan.

A. GDI Cell Functions:

The GDI strategy depends on the utilization of a straightforward cell as appeared in Fig. 2. At first look, the

essential cell helps one to remember the standard CMOS inverter, yet there are some imperative contrasts.

- The GDI cell contains three inputs: G (normal entryway info of NMOS and PMOS), P (data to the source/channel of PMOS), and N (information to the source/channel of NMOS).
- Bulks of both NMOS and PMOS are associated with N or P (separately), so it can be subjectively one-sided at stand out from a CMOS inverter.

It should be commented that not the majority of the capacities are conceivable in standard p-well CMOS prepare however can be effectively executed in twin-well CMOS or silicon on protector (SOI) advances. Table 4.1 demonstrates how a straightforward change of the data setup of the basic GDI cell relates to altogether different Boolean capacities. The majority of these capacities are mind boggling (6–12 transistors) in CMOS, and additionally in standard PTL executions, however extremely straightforward (just two transistors for every capacity) in the GDI plan technique.

In this paper, the greater part of the composed circuits depended on the first and second capacities. The purposes behind this are as per the following.

F1 and f2 yields are finished rationale families (permits acknowledgment of any conceivable two-data rationale work). F1 is the main GDI work that can be acknowledged in a standard p-well CMOS prepare, on the grounds that the majority of any NMOS is always and similarly one-sided. When N data is driven at high rationale level and P information is at low rationale level, the diodes in the middle of NMOS and PMOS masses to Out are straightforwardly enraptured and there is a short in the middle of N and P, bringing about static power dispersal and.

S.No.	N I/P	P I/P	G I/P	Output	Function
1.	0	B	A	A'B	F ₁
2.	B	1	A	A'+B	F ₂
3.	1	B	A	A+B	OR
4.	B	0	A	AB	AND
5.	C	B	A	A'B+AC	MUX
6.	0	1	A	A'	NOT

Fig. 3: Logic Functions of Basic Gate-Diffusion-Input Cell.

IV. IMPLEMENTATION OF 2X1 AND 4X1 MULTIPLEXER USING GDI

Multiplexer is an advanced circuit. The basic MUX has quantities of information input-lines and one output. The choice of a specific information input is taken by an select-line. It has 2n info-inputs and n determination output-lines which bit blends figure out information is chosen. Figure-5.3 demonstrates execution of fundamental 2x1multiplexer utilizing Gate-Diffusion-Input circuit. The 4-by-1 MUX having 4-inputs, 2-determination input-lines and one output-line. Contingent upon the two-choice, one yield is chosen at once among the four information-lines. Fig.5.4 indicates execution of 4x1multiplexer utilizing Gate-Diffusion-Input circuit.

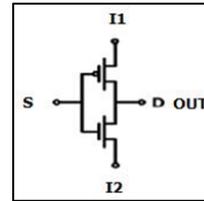


Fig. 4: GDI based 2x1 Multiplexer

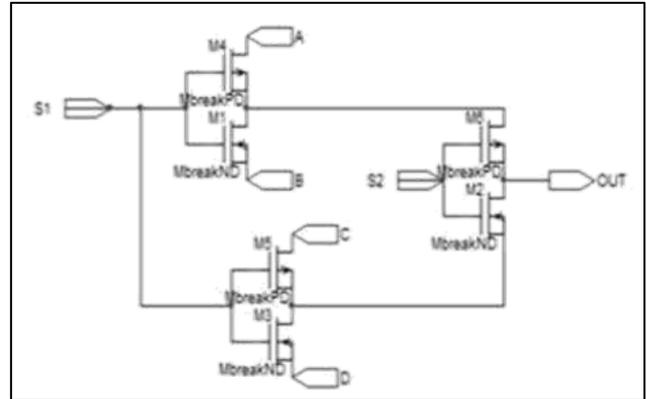


Fig. 5: GDI based 4x1 Multiplexer

N	P	G	OUTPUT	FUNCTION	TRANSISTOR COUNT
0	1	A	A'	Inverter	2
0	B	A	A'B	F ₁	2
B	1	A	A'+B	F ₂	2
1	B	A	A+B	OR	2
B	0	A	AB	AND	2
C	B	A	A'B+AC	MUX	2
B'	B	A	A'B+B'A	XOR	4
B	B'	A	AB+A'B'	XNOR	4

Table 1: Gate-Diffusion-Input circuit with its various-operations

V. THE STRUCTURE OF PROPOSED LOW-POWER GATE-DIFFUSION-INPUT FA DESIGNED WITH MUX

The below figure illustrates how a 2:1 MUX can be designed by using Gate-Diffusion-Input Cell. The PMOS and NMOS transistors are connected as inverter as shown in the below figure. The gate of both PMOS and NMOS is shorted and connected as SELECT line (A) of 2:1 MUX. The source of the PMOS is used as input (P) line and source of the NMOS is used as another input line (N). As we know that, the PMOS turns on when a low input is given and NMOS turns on when a high is given.

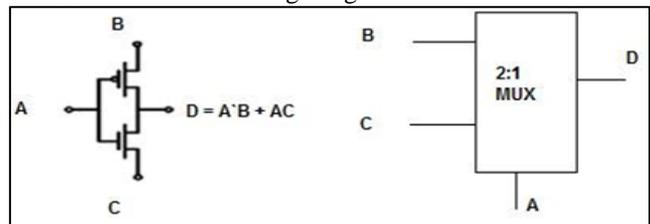


Fig. 6: 2:1 MUX design using two transistors

When the gate input is low, the input at line P is selected and observed at output D. on the other hand when the input is high; the data at line N is selected and observed at output D.

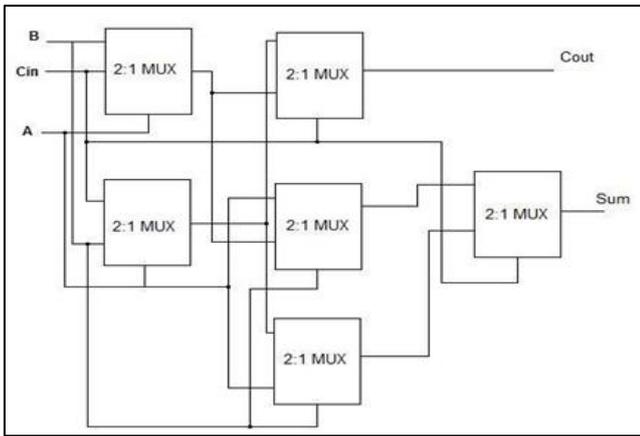


Fig. 7: Block Diagram of Low Power Proposed Full Adder using 2T MUX

The above figure shows the proposed single bit full-adder using 2-transistor MUX. Here 6 MUXs connected to get full-adder output. Now it totally requires 12 transistors to design Full-Adder.

VI. SIMULATION

The simulation tools are used to understand the behavior of abstract circuits based on given inputs. Simulation tools can be used to study the behavior and timing diagrams of the proposed circuit. The conventional full-adder and our proposed twelve-transistor full-adder are studied in a simulation tool using 90nm technologies. The conventional FA with 28-transistors is implemented and simulated for its power usage and timing waveforms. Later the low power full-adder is designed & simulated. This proposed adder is implemented with 2-transistor multiplexer.

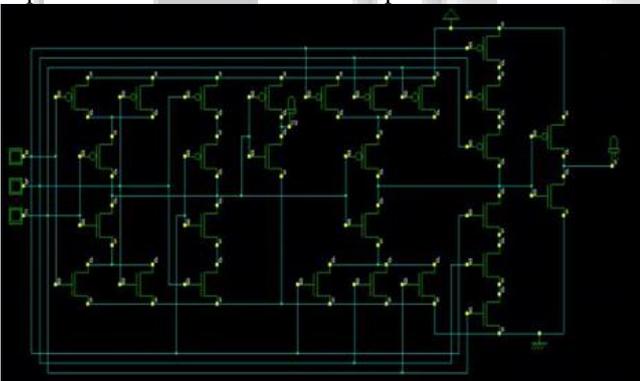


Fig. 8: Schematic of 28-transistor CMOS-FA

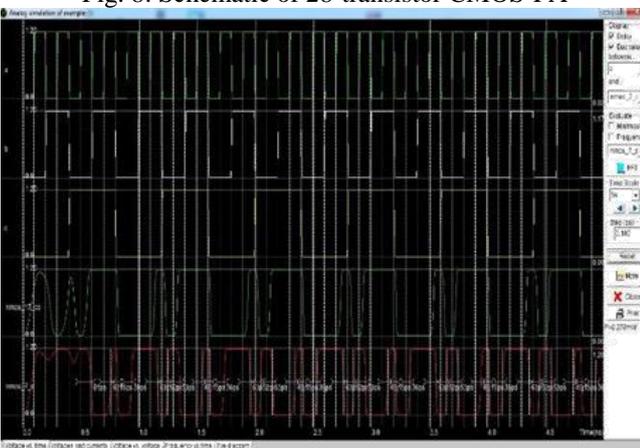


Fig. 9: Output waveforms of 28-transistor FA

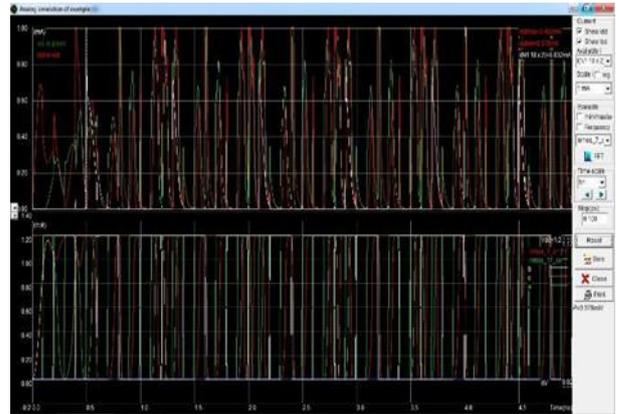


Fig. 10: Output of 28-transistor FA [voltage v/s current]

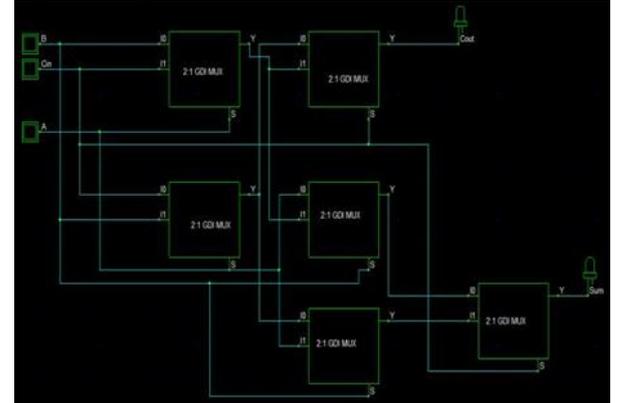


Fig. 11: Schematic of proposed-FA with Multiplexer

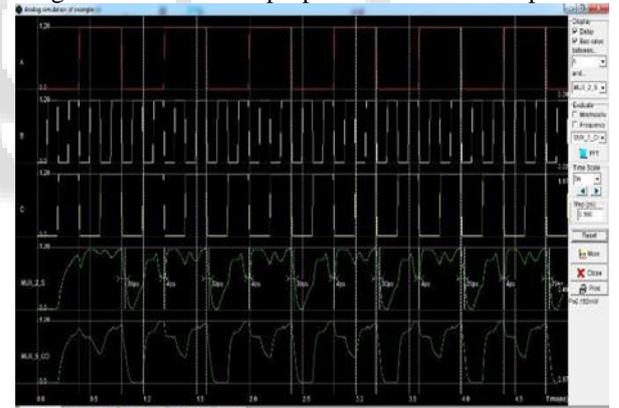


Fig. 12: Waveforms proposed FA

VII. RESULTS FROM SIMULATION

	Conventional FA with 28-transistor	GDI FA with MUX
Power Analysis	0.378 mW	0.185 mW
Delay analysis	Tr=63 ps	Tr= 4 ps
	Tf=15 ps	Tf= 36 ps
	Td(avg)=39 ps	Td(avg)= 20ps

Table 1: Results

VIII. CONCLUSION

It can be seen that, from the above discussion & results, the proposed GDI Full-adder is better in operation speed and consumes less energy compared to other conventional adders. Clearly it can be mentioned that this adder can be used to implement complex operations also.

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