A Bridgeless Buck Boost Converter Based Multiple Output SMPS to Improve Power Quality

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Abstract— This paper deals with the design, simulation and development of power factor correction (PFC) with the multiple output switched mode power supply (SMPS) using the back to back connected buck boost converter. Ac supply is fed to the back to back connected buck boost converter to eliminate a diode bridge rectifier used in real time, which result in power quality improvement. The operation of buck boost converter in discontinuous conduction mode ensures efficient power factor correction and reduces complexity in control. And additional ac source is fed to multi terminal transformer to supply ac when PV fails. The performance of proposed system is evaluated by connecting varying input voltages and it is simulated in MATLAB/Simulink environment. The simulation results ensures the improvement in the performance of proposed SMPS.

Key words: Bridgeless Buck Boost Converter, Multiple Output Switched Mode Power Supply (SMPS), Power Factor Correction (PFC)

I. INTRODUCTION

Switched mode power supplies (SMPS) normally uses diode bridge rectifier (DBR) followed by the filter capacitor to supply the multiple output dc voltage used in personal computer. The DBR causes deterioration in power quality[1],[2], and it results in very low power factor and high harmonic at input side. To achieve the better reliability and efficiency the power factor correction (PFC) circuits are employed at the utility interface,[2],[3]. Even in fluctuating input voltages PFC is able to achieve low THD and high PF and also provide stiffly output dc voltages. The recent development of bridgeless single ended primary inductance converter and cuk converter replaces the DBR which results in low voltage stress, low conduction loss[4]-[6]. But it has some disadvantage that component count is high so its not suitable for low power SMPS applications. A bridgeless buck PFC converter and bridgeless boost converter is reported in,[7],[8] which eliminate one diode drop in current circuit and also output voltage range has some violation limit. A buck–boost converter configuration is best suited for computer SMPSs apart from various bridgeless converter topologies because it can handle a larger voltage range and yet deliver stiffly regulated output voltages [9]. Though one of the switches device always on conduction [10], which results in conduction losses. Instead of using the unipolar converter we use half bridge VSI because of better core utilization,[11]-[14]. The bridgeless converter-based multiple-output SMPS has been particularly targeting SMPSs for PCs in order to reduce current harmonics and high PF.

A. Bridgeless Converter Based Multiple Output Configuration

The proposed system configuration is shown in Fig 1.

A AC supply is fed to the bridgeless buck boost converter with MOSFET switches and two diodes the gate pulses to the switch is given by the pulse generator. Both the inductors on buck boost is designed to operate in discontinuous conduction mode. Then the regulated dc output voltage are fed to the half bridge VSI to obtain multiple dc voltages. The half bridge VSI consist of two input terminal and multiple output voltage transformer which are connected in center tapped configuration to reduce losses. Ac source is connected to the one input terminal of the HFT along with breaker circuit. Once the pv fails or unable to supply the ac supply provide supply to transformer. By setting the breaker time we can control the the operation. On the secondary side of the the HFT multiple dc output voltage is achieved through the filter inductors L1, L2, L3, L4 and capacitors Co1, Co2, Co3, and Co4 are connected to reduce the current and voltage ripples respectively. The effect of varying input voltages and loads is studied to reveal the improved performance of the proposed bridgeless-converter-based multiple-output SMPS.

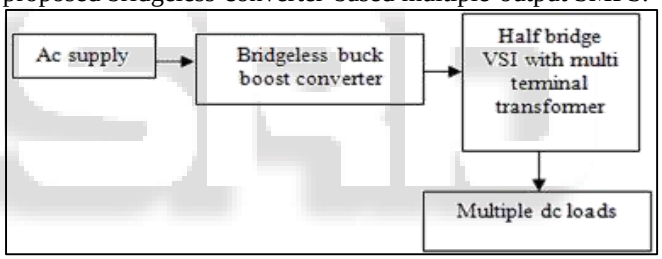

Fig. 1: proposed system configuration

B. Operating Principle of Proposed System

The proposed bridgeless-converter-based multiple-output SMPS consists of a AC feeding two back to-back-connected buck–boost converters with a half-bridge VSI and multiple-output HFT at the load end. The buck–boost converters are controlled suitably to obtain a high PF and low input current THD. The half-bridge VSI at the output takes care of high-frequency isolation with multiple dc output voltages being regulated. The operation of both converters in one switching cycle is described in the following subsections

The ac supply is fed to the buck boost converter contains the MOSFET switches diodes and parallel capacitor in which the gate pulses are given to the switches with the help of pulse generator . The buck–boost converter is a type of DC-to-DC converter that has an output voltage magnitude that is either greater than or less than the input voltage magnitude. The output voltage is typically of the same polarity of the input and can be lower or higher than the input. Such a non-inverting buck-boost converter may use a single inductor which is used for both the buck inductor and the boost inductor.

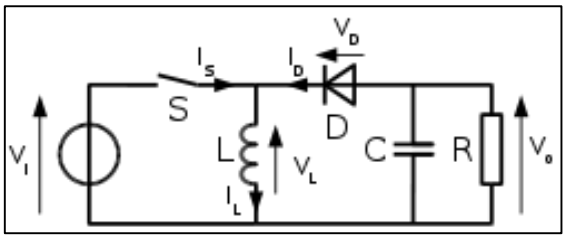

Fig. 2: Schematic diagram of buck boost converter

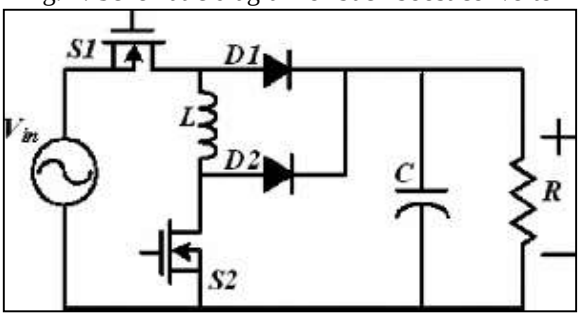

Fig. 3: Schematic Diagram of Bridgeless Buck Boost Converter

The controlled output dc voltage of the dual buck–boost converter is fed to the half-bridge VSI for high-frequency isolation, for voltage scaling, and for obtaining multiple dc output voltages. The operation of the half-bridge VSI in one switching cycle is described in four states. Operating modes for under (a) upper switch *Sp* is on, (b) upper switch *Sp* is off, (c) both switch and diode are off, and (d) waveforms in one switching cycle fourth states are similar and occur twice in each switching cycle, as shown in Fig. 4(b). In the first state, the upper switch *S*1 is turned on; the input current circulates through the primary winding of the HFT to the lower input capacitor *C*12. Diodes *D*1, *D*3, *D*5, and *D*7 start conducting, and the inductors associated with the windings start storing energy, as shown in Fig. 4(a). Therefore, inductor currents *iL*1, *iL*2, *iL*3, and *iL*4 increase, and output filter capacitors *Co*1, *Co*2, *Co*3, and *Co*4 discharge through the loads. In the second state [Fig. 4(b)], both switches are turned off, and all secondary diodes *D*1–*D*8 freewheel the stored energy until the voltage across the HFT becomes zero. Therefore, inductor currents *iL*1, *iL*2, *iL*3, and *iL*4 start decreasing. In the third state of the switching cycle, the second switch *S*2 is turned on, and the input current flows through upper capacitor *C*11 and the primary winding, as shown in Fig. 4(c). Associated diodes *D*2, *D*4, *D*6, and *D*8 in the secondary windings conduct, and inductors *L*1, *L*2, *L*3, and *L*4 start storing energy. When the energy stored in the inductors reaches maximum values, the switch is turned off. In the last state, all secondary diodes start conducting, which is similar to the second state. The same operating states repeat in each switching cycle

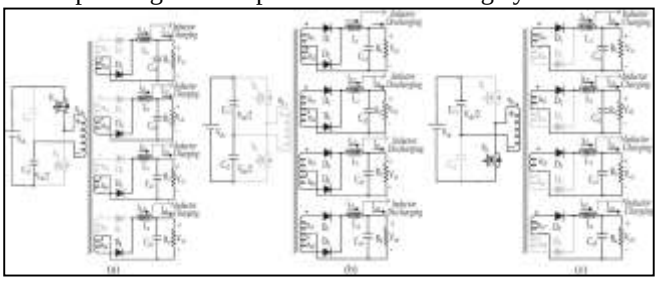
Fig. 4: (a) When the first switch *S*1 is on, (b) when both switches are off, (c) when the second switch *S*2 is on
Simulation And Test Results

This section explains the detailed simulation results of the proposed system. The simulated system is shown in Fig.4. MATLAB/SIMULINK tool is used for simulation studies.

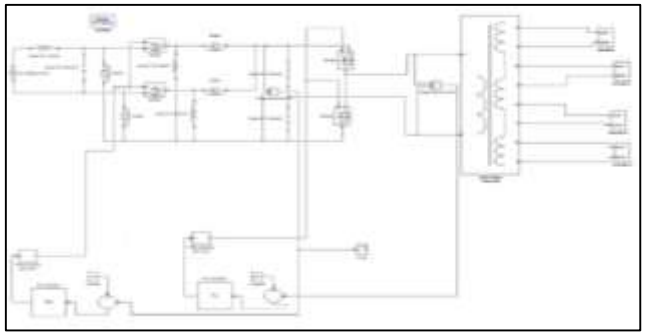
Fig. 5: MATLAB model for the multiple output SMPS with PV

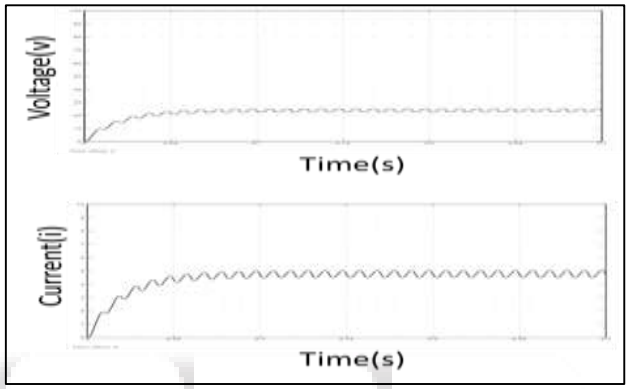

Fig. 6: Graphical representation of output dc voltage [V=24V] and current [I=5A]

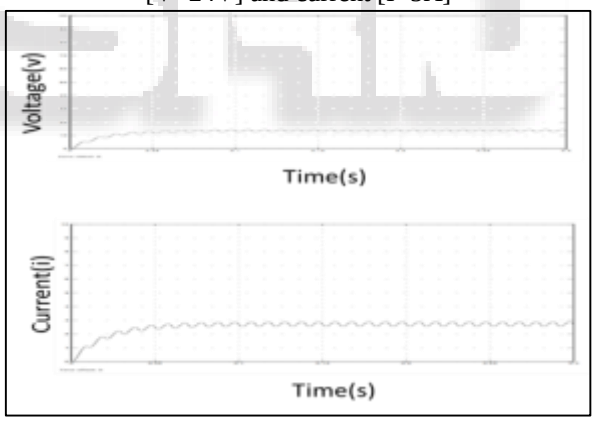

Fig. 7: Graphical representation of output dc voltage [V=14V] and current [I=2.8A]

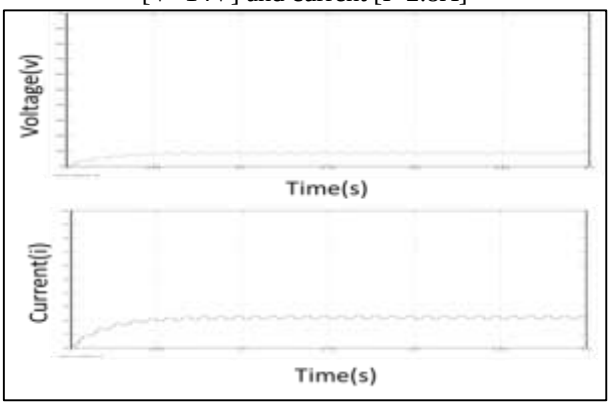

Fig. 8: Graphical representation of output dc voltage [V=12V] and current [I=2.2A]

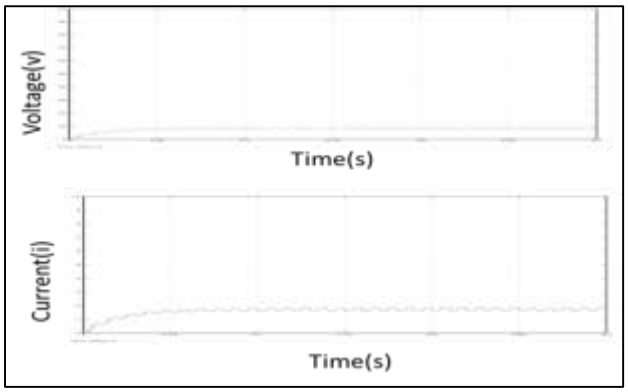

Fig. 9: Graphical representation of output dc voltage [V=8V] and current [I=1.8A]

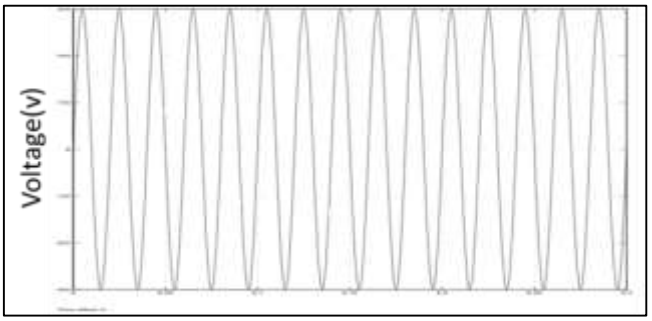

Fig. 10: Graphical representation of input ac voltage [v=300v]

Input voltage	Power factor	Input current
170v	0.9994	2.17
220v	0.9989	1.68
270v	0.9986	

Table.1 power quality indices

II. CONCLUSIONS

A bridgeless-converter-based multiple-output SMPS has been designed, simulated, and implemented in hardware to demonstrate its capability to improve the power quality at the utility interface. The output dc voltage of the first-stage buck–boost converter has been maintained constant, independent of the changes in the input voltage and the load. A satisfactory performance has been achieved during varying input voltages and loads with power quality indices remaining within the acceptable limits set by IEC 61000-3-2. The proposed SMPS has shown satisfactory performance, and hence, it can be recommended as a tangible solution for computers and other similar appliances

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