User Controlled, Hardware Approach to Multi Byte Convolutional Encoder

Bhaskar Nandy
M. Tech Scholar
Department of Electronics & Communication Engineering
Heritage Institute of Technology, West Bengal, India

Abstract— This paper focuses on Field Programmable Gate Array (FPGA) which is designed to user operate as an non systematic, convolutional encoder with its best performance configuration with a code rate of 0.5 and constraint length 3. BPSK is modulation technique which is implemented for this system which is analyzed to be the best modulation technique so far. Errors do occur randomly in any communication system is the most concerning factor since it makes the system vulnerable to security threats. A system being designed to prevent such treats by detecting, amending the errors as far as possible. Convolutional codes is a supreme forward error correcting (FEC) code with a least code rate which serves this purpose.

Key words: FPGAkitBasys2board;Xilinx ISE design suite 14.1;MATLAB & SIMULINK verR2013a; MATLAB Communication Tool box; Code Rate; Constraint length; Generator Polynomial; Poly2trellis structure

I. INTRODUCTION

'Convolutional codes were invented by Peter Elias in the year 1955[1] .Convolutional codes belong to the FEC(Forward Error Correcting) scheme. Convolutional encoding is a process of channel coding. BPSK is the best modulation scheme. Later on Jack Wozencraft recognized that the tree structure of convolutional codes [2]. Then in the year 1967, Andy Viterbi introduced Viterbi algorithm (VA) as an "asymptotically optimal" decoding algorithm for convolutional codes [3]. Ever since then, Convolutional coding with Viterbi decoding has been the prominent forward error correction technique used in Satellite Communication.'

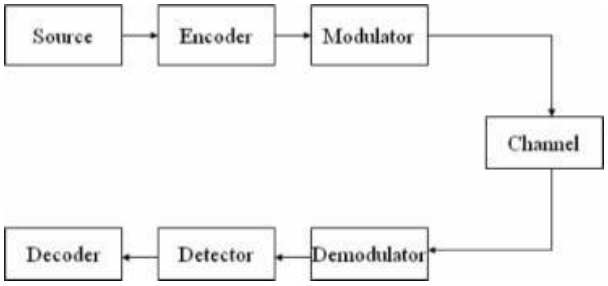

Fig. 1: Convolutional encoder/decoder position in a digital communication system

A. Convolutional Code

We know that (n,k) block code where code words are constructed independently of each other. Convolution code differ from block codes in the encoder output that is to say, it is not constructed from single input but by using, previous encoder input bits. Clearly memory registers are required to store the input for future use. Code rate of convolutional code, is calculated as k/n which also defines the efficiency of the code ,while quantity L is called the constraint length of code which is defined as no. of shifts over which a single message bit can influence the encoder outputs. calculated as L = m+1. where, 'm' denotes no. of memory elements used, 'n' denotes no. of outputs and 'k' denotes no. of inputs to the encoder. So, Fig 2 suggests a Code Rate of 0.5 & Constraint Length of 3.

B. Convolutional Encoder

The block diagram of convolution encoder is shown in Fig 2.To generate the output, the encoder uses three values of the input signal, one present and two previous input values. The set of past values of input data is called a state. Each set of outputs is generated by EX-OR-ing a pattern of current and shifted values of input data. Here (so,s1,s2) are memory states of the shift register. First coded bits and Second coded bits are outputs as(C1,C2) [4].

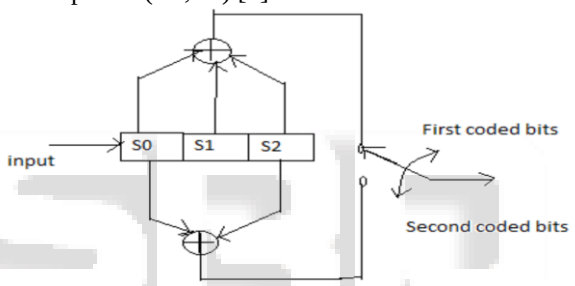

Fig. 2: Block diagram of (2,1,3) convolutional encoder

C. Generator Polynomial

A polynomial forming the generator polynomial should be at most K degree and specifies the connections between the shift registers and the modulo-2 adders or EXOR gates.

Two generator polynomials are $g1(x) = 1+x^2$, $g2(x) = 1+x+x^2$ which give g1(x) = (101) and g2(x) = (111) [4].

D. Poly2trellis Structure

It converts convolutional code polynomials to trellis description and the format is: (L,[g2,g1]) where values of g1,g2 are in octal bases. So according to Figure2,we can say its poly2trellis(3,[7,5]) for the above configuration [4].

E. Mode of Selecting The Polynomials

These are good and efficient polynomials found in this list usually found by simulation. These polynomials proved to have good performance.

CONSTRAINT LENGTH	G1	G2
3	101	111
4	1101	1110
5	11010	11101
6	110101	111011
7	1011011	1111111
8	11011111	11100111
9	110111101	111001101
10	1100111001	1110011001

Table 1: Generator Polynomials for good rate 1/2 codes

II. IMPULSE RESPONSE

An encoder can be accessed on the basis of its impulse response. Impulse response is that response of the encoder when a single '1' bit or '0' bit is passed through it. Consider the contents of the register shown in table as a '1' moves through it [4].

Memory states Contents	**Output(C1)**	**Output(C2)**
1 0 0	1	1
0 1 0	1	0
1 0 1	0	0
0 1 0	1	0
1 0 1	0	0
0 1 0	1	0
1 0 1	0	0
0 1 0	1	0

Table 2: Impulse Response of the (2,1,3) Encoder for a byte of information

A Byte of message bits is encoded by the encoder.
Input :10101010.
Output:11 10 00 10 00 10 00 10.

A. Encoder Operation

The encoding of the 8-bits input sequence [1 0 1 0 1 0 1 0], a byte of information for the 8 sequential time periods is as shown in Fig 3.

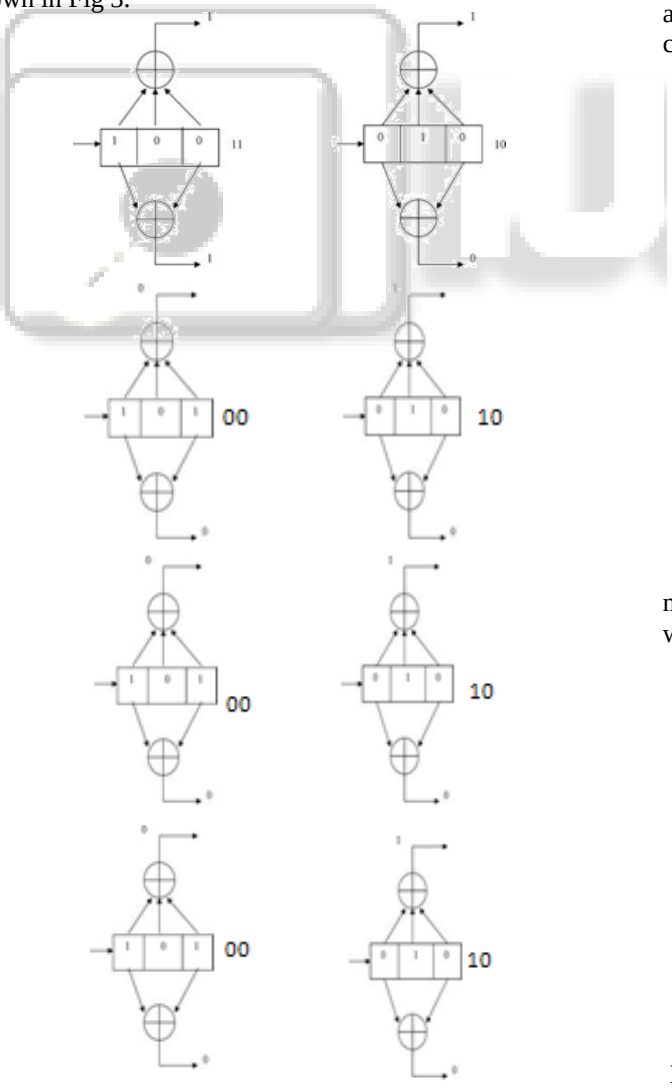

Fig. 3:

Time	Input Bits	Output Bits	Encoder Bits
0	1	1 1	0 0
1	0	1 0	1 0
2	1	0 0	0 1
3	0	1 0	1 0
4	1	0 0	0 1
5	0	1 0	1 0
6	1	0 0	0 1
7	0	1 0	1 0

Table 3: Result showing the working of a (2, 1, 3) Convolutional Encoder for a byte of information

A Byte of message bits is encoded by the encoder.
Input :10101010.
Output:11 10 00 10 00 10 00 10.

B. Different Encoder Configurations For The Fixed Constraint Length *3*

It has been observed that three different encoder circuits can be formed. We are differentiating them with poly2trellis structure.

1) Poly2trellis(3,[7,4]); implies g2(x)=111,g1(x)=100;
2) Poly2trellis(3,[7,5]); implies g2(x)=111,g1(x)=101;
3) Poly2trellis(3,[7,6]); implies g2(x)=111,g1(x)=110;

BER analysis is first done to obtain the best modulation type for the circuit. Then we have extended our analysis to find the best performing circuit so that hardware can be configured with it [4].

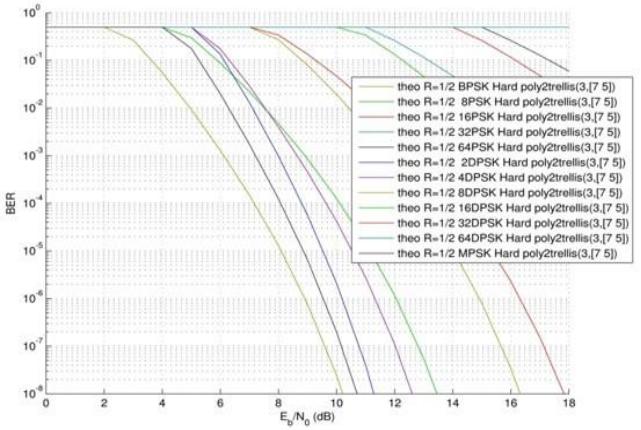

Fig. 4: Comparison Between Different Modulation Techniques

It is found that for a constant BER, BPSK modulation technique performs best modulation process with lesser energy required to transmit the bits.

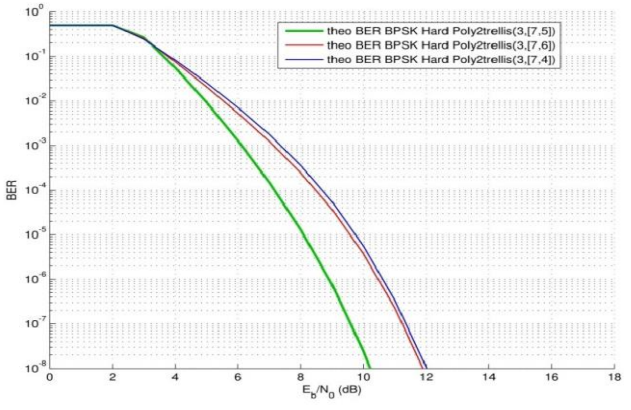

Fig. 5: Comparison between different circuit configurations

Out of these circuits, for a constant BER, the circuit with poly2trellis(3,[7,5]) has the best performance. This indicates we need to have an encoder circuit with three memory elements and g2= (111) and g1= (101) as their impulse response.

C. Encoder Design

As we came to know about the circuit configuration we tried to implement it with Xilinx ISE Design Suite 14.1 with Verilog programming.

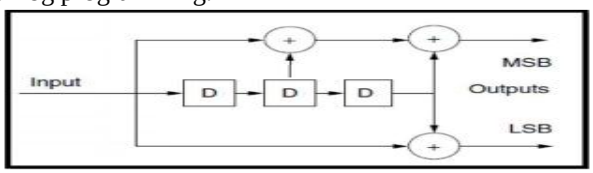

Fig. 6: Blockdiagram for the proposed design(Non-Recursive, Non Systematic Convolutional Encoder (2, 1, 3))

ENCODER PARAMETERS	DESCRIPTION
Rate of the encoder	1/2
Constraint length of the encoder	3
Number of inputs	1 bit input at a time
Generator polynomials	[1 1 1] [1 0 1]

Table 4: Hardware Description for the convolutional encoder

D. Verilog Program For Top Level In ISE Design Suite [5,6]

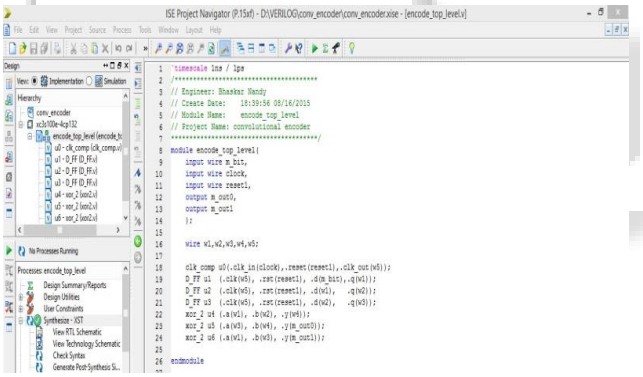

Fig. 7: Program After Synthesis

E. UCF(User Constraint File) File Created For User Input

```
"Port mapping for the ports to be used by the user."
NET "m_out0" LOC = M11;  //Output LED "LD01"
NET "m_out1" LOC = M5;   //Output LED "LD00"
NET "m_bit" LOC = P11;   // Input "SW0"
NET "clock" LOC = B8;    //Master clock
NET "reset1" LOC = A7;   //Reset input "BTN3"
```

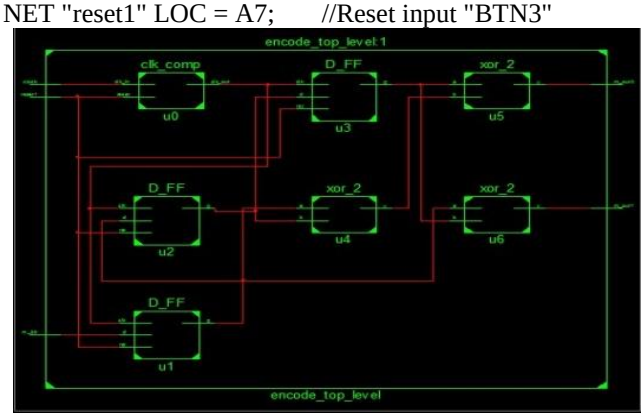

Fig. 8: RTL Schematic Of The Proposed Design

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	32	1,920	1%	
Number of 4 input LUTs	38	1,920	1%	
Number of occupied Slices	37	960	3%	
Number of Slices containing only related logic	37	37	100%	
Number of Slices containing unrelated logic	0	37	0%	
Total Number of 4 input LUTs	65	1,920	3%	
Number used as logic	38			
Number used as a route-thru	27			
Number of bonded IOBs	5	83	6%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	2.14			

Fig. 9: Device Utilization Summary.

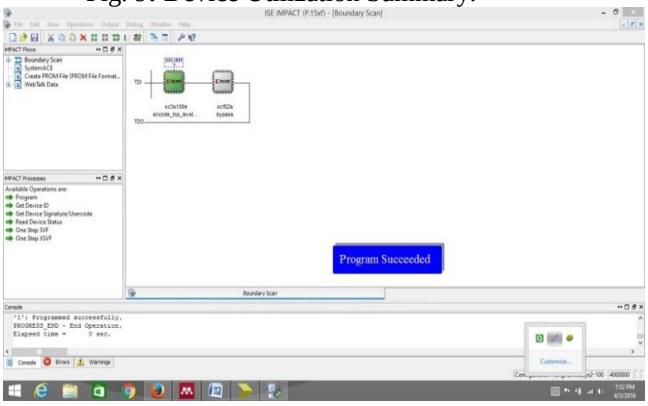

Fig. 10: Program burned to FPGA kit (BASYS 2 XCS100E).

F. User Defined Inputs Are Given As Follows

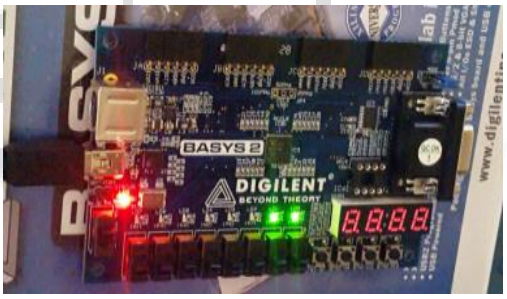

Fig. 11: OUTPUT >11when INPUT>1 ; t=0

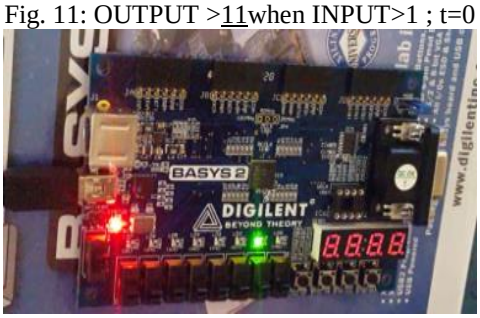

Fig. 12: OUTPUT >10 When INPUT>0; T=1

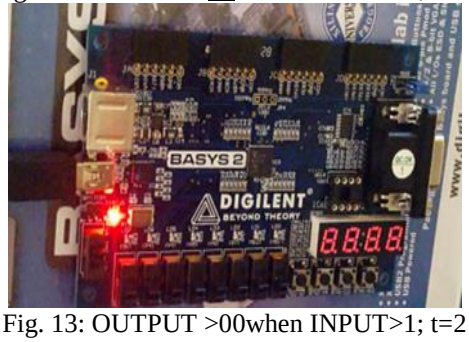

Fig. 13: OUTPUT >00when INPUT>1; t=2

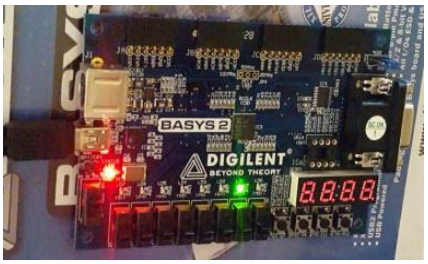

Fig. 14: OUTPUT >10 when INPUT>0; t=3

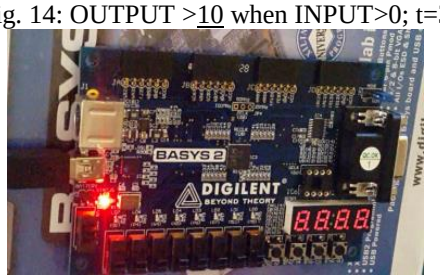

Fig. 15: OUTPUT >00when INPUT>1; t=4

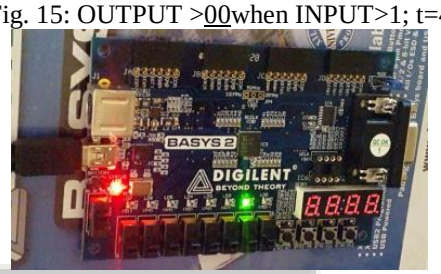

Fig. 16: OUTPUT >10 when INPUT>0; t=5

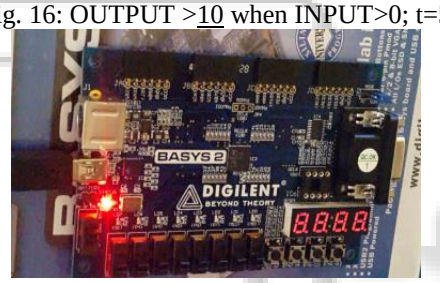

Figure 17: OUTPUT >00when INPUT>1; t=6

Fig. 18: OUTPUT >10 when INPUT>0; t=7

A Byte of message bits is encoded by the encoder.
Input :10101010.
Output:11 10 00 10 00 10 00 10 is obtained as shown in the above figures and it matches with the theoretical values.

III. Conclusions

From BER (Bit Error Rate) analysis we have found that the BPSK modulation technique is the best modulation technique to transmit bits with lesser energy. BER plot also showed us the best circuit to implement with the hardware i.e. Poly2trellis(3,[7,5]). The device utilization summary of Basys 2 FPGA kit for the concerning encoder, suggests that it occupies very less space to fabricate this system on chip (SOC) so indirectly it would cost very less.

References

[1] P. Elias, “Coding for noisy channels,” IRE Conv. Rec., pt. 4, pp. 37–46, Mar. 1955. Reprinted in Key Papers in the Development of Information Theory (D. Slepian, ed.), IEEE Press, 1973; Key Papers in the Development of Coding Theory (E. R. Berlekamp, ed.), IEEE Press, 1974; The Electron and the Bit (J. V. Guttag, ed.), EECS Dept., MIT, Cambridge, MA, 2005.
[2] J. M. Wozencraft and B. Reiffen, Sequential Decoding. Cambridge, MA: MIT Press, 1961.
[3] Viterbi.A.J, "Convolution codes and their performance in communication systems," IEEE Transaction on Communications, vol.com-19, pp. 751 to 771, October 1971.
[4] Bhaskar Nandy,"Analysis of Convolutional Encoder System" International Journal of Current Engineering and Technology (ISSN: 2277 – 4106) in Vol.6, No.2 (March/April 2016) at page no. 590-595
[5] Samir Palnitkar, "Verilog HDL: A Guide to Digital Design And Synthesis, Second Edition", PHP.
[6] Hardware Implementation of Viterbi Decoder for Wireless Applications Bhupendra Singh, Sanjeev Agarwal2 and Tarun Varma3,Deptt. of Electronics and Communication Engineering ,Amity School of Engineering and Technology, Noida, India International Journal of Computer Communication and Information System (IJCCIS)– Vol2. No1. ISSN: 0976–1349 July – Dec2016.

