Approximate Mode of Wallace Tree Multiplier using Adiabatic Logic on Fin-FET for Video-Encoding

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Abstract— Approximate computing has been gaining momentum over the past few years with progressive research particularly in applications exercising signal processing techniques. Human imperceptibility could be taken advantage of by some image and video compression standards such as JPEG and MPEG which have tolerance to computing imprecisions that yields an algorithm possessing power efficiency. With hardware approximations that are often statistically fixed, the prevailing architectures are not very efficient in adapting to different inputs, like in the case of MPEG coder whose output quality varies significantly for different input videos due to their fixed approximation hardware configurations. This paper faces the above mentioned issue by proposing a reconfigurable approximate architecture for MPEG encoders. This is achieved by designing arithmetic unit using Adiabatic Vedic alias low power high speed technique that with a FinFET device. Further, low area overhead helps in solving the issues prevalent in conventional design, like power variant, and speed up-gradation, area consumption. Low power and high speed CLA have to be designed using adiabatic Vedic gates (EEAL), followed by the Arithmetic unit (Multiplier) which must be implemented using the Proposed Adiabatic Vedic CLA. The overall architecture has sufficient energy, power consumption reduced delay architecture and saves area which enhances its utility value.

Key words: Adiabatic Logic, Video-Encoding

I. INTRODUCTION

Various concepts on all hierarchical levels have been proposed in the past to decrease active losses in static CMOS circuits. Active losses are represented by αCV2DD, where VDD is the power supply, C the capacitance of the circuit, and α is activity factor. Hence the most effective way to decrease active losses is reducing the voltage. Voltage scaling helps to cut-down active losses, and on the downside the gate delay is increased. The capacitance is determined by the intrinsic capacitance of the devices in the applied technology, and the parasitic capacitances due to interconnects, that can be minimized by compact layout of integrated circuits. Activity can be brought to minimal by avoiding unnecessary switching losses due to glitch, but also by applying algorithms that apply less power consuming operations. Additional power consumption in synchronous designs is fulfilled by clock tree. With a high activity factor these losses can add up to 50% to the overall losses for high-performance microprocessors. Clock-gating can avoid those losses, flip flops and clock branches are disconnected from the clock tree for inactive circuits.

Passive losses due to leakage currents gain more importance with on-going shrinking of microelectronic circuits. Power-gating cuts off unused circuits from the power supply. Uncritical paths within a complex system can be provided with higher Vth devices, thus allowing for a trade-off of speed for passive losses. Besides those circuit level methods to cut down leakage losses, new transistor concepts are also presented to cope with leakage losses.

The Fin-Shaped Field Effect Transistor (Fin-FET) as well as the Carbon Nanotube (CNT) based field effect transistor are promising concepts that can draw new limits and boundaries to miniaturization in integrated circuit design.

Adiabatic Logic has proven to be a circuit technique with the potential to dramatically decrease the energy consumed per operation. Investigations on the gate level have projected a major cut-down of losses with respect to static CMOS is gained. The previous work concluded that out of the broad variety of adiabatic gate topologies, only a few are liable successors to static CMOS, as those are compatible to a static CMOS design flow, are robust with respect to PVT variations, and apply a manageable number of clocked power-supplies that can be generated in an energy efficient manner.

II. ADIABATIC LOGIC WITH FINFET

The Fin Shielded Field Effect Transistor (FinFET) is a proposed, novel 4 terminal device with a source, a drain, and two gate. Its geometry is based on cylindrical elements of radius r as pictured in Fig.3.1 and is regarded as a hybrid of a JFET and a MOSFET device. Majority carriers transport charge through the bulk. Two gates control depletion regions into the bulk, thereby controlling the channel width. Compared to a JFET a MOS structure for the gates is found wherein the gates are separated from the bulk via an oxide. Gate leakage currents are expected to be negligible compared to a JFET device, since tunnelling currents account for the gate leakage in comparison to junction leakage in JFET devices. Parameters to adjust are the thickness tox of the gate oxide, and the doping concentration in the channel region.

Various configurations are possible for the FinFET device, as the two gates can be controlled independently. Tied configuration, where both gates are connected and controlled by the same signal, and independent gate, that allows controlling the depletion regions from both sides independently. The independent gate control allows for the integration of the non-trivial logic functions AND and OR within one device.

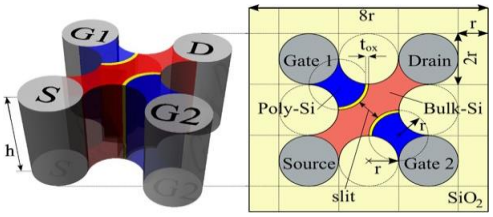

Fig. 2.1: Basic structure of a Fin Shielded Field Effect Transistor (FinFET) in a 3D and the top view.

III. STATIC AND ADIABATIC MULTIPLIER USING FINFET

A. Adiabatic Logic Gates

Adiabatic circuits are low power circuits which use "reversible logic" to conserve energy. The term comes from the fact that an adiabatic process is one in which the total heat or energy in the system remains constant. Adiabatic Gates are driven by any combination of 2 inputs and its output driven capability of 2 mode of operation at the same time. So the total area occupied is less compared to conventional CMOS logic gates. Moreover power and delay factors are considerably achieved over existing CMOS based gates. There are several adiabatic logic gates are present, such as follows 1)ECRL 2)EEAL

1) ECRL adiabatic logic

Efficient charge recovery logic adopts a new method that performs precharge and evaluation simultaneously. ECRL eliminates the precharge diode and dissipate less energy than other adiabatic circuits. This logic has the same circuit structure as cascade voltage switch logic or DCVS with differential signalling.

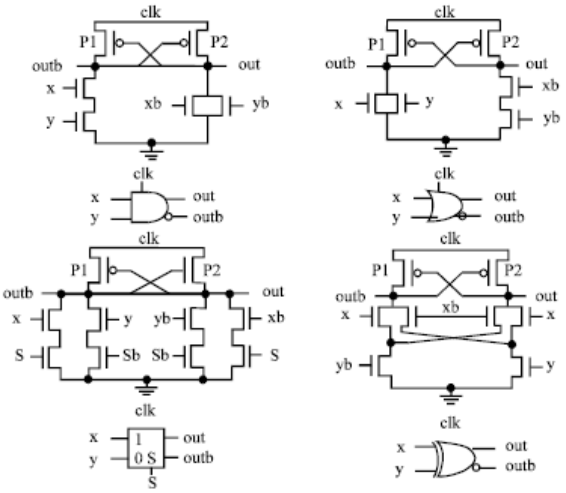

Fig. 2.2:

2) EEAL adiabatic logic

EEAL is a dual-rail adiabatic logic consisting of two DCVS network and a pair of cross-coupled PMOS devices in each stage. EEAL runs on only one sinusoidal power clock supply, has simple implementation, and an enhanced performance compared with previously proposed adiabatic logic families in terms of energy consumption.

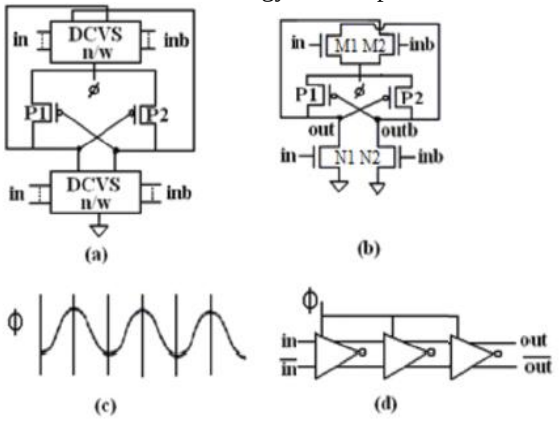

Fig. 2.3:

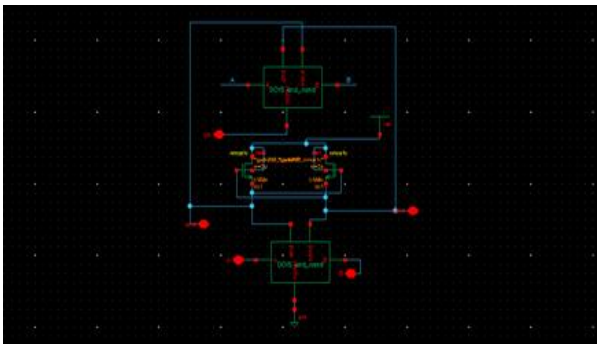

Fig. 2.4: EEAL And/Nand gate

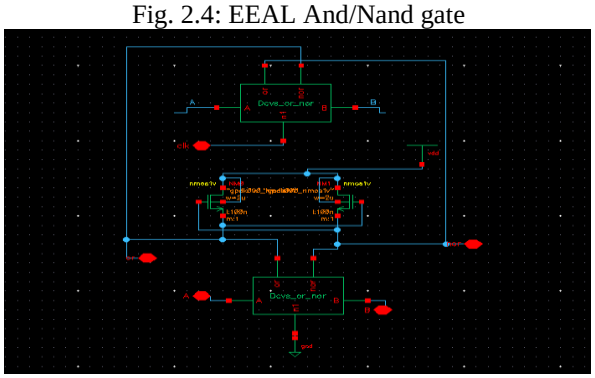

Fig. 2.5: EEAL OR/NOR gate

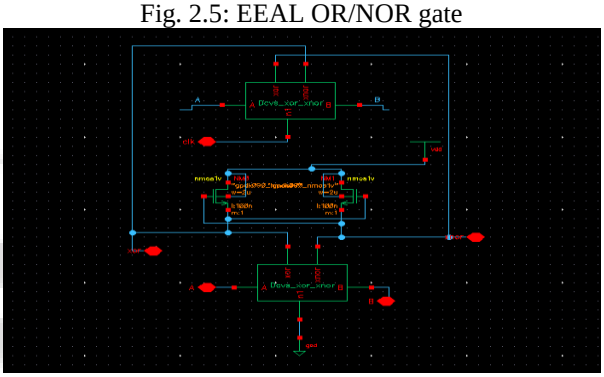

Fig. 2.6: EEAL XOR/XNOR gate

B. 4x4 Wallace Tree Multiplier Architecture

A 4bit * 4bit booth-encoded Wallace tree multiplier is implemented in Verilog to demonstrate the proposed multiplier. The Wallace tree part of the multiplier is shown in the figure.

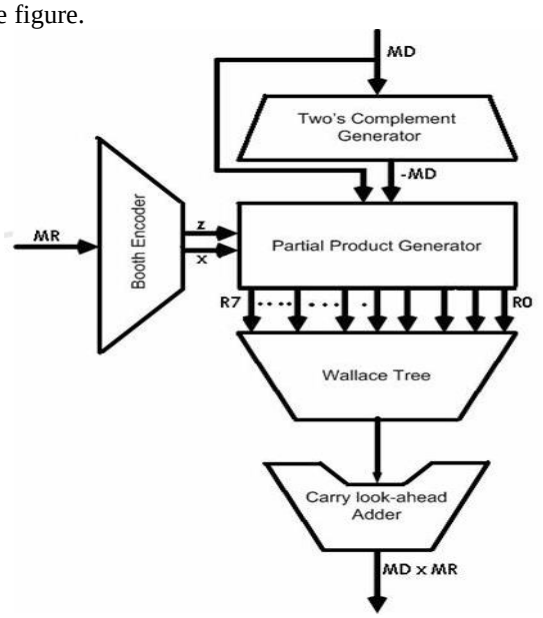

Fig. 2.7:

C. Description Of Architecture

The multiplier (MR) and the multiplicand (MD) are two 8 bit operands, and at its output it produces the 16-bit multiplication result of the two 8bit operands. The multiplier architecture primarily consists of five major modules. They are: 2's Complement Generator, Booth Encoder, Partial Product Generator, Wallace Tree and Carry Look-ahead Adder. The multiplier has been constructed in simplest form. We have used original Booth's Algorithm (Radix 2 encoding) for the Booth Encoder. Ripple Carry Adder constructed from Full-adder modules is used in the 2's Complement Generator. Two control signals x and z produced by the Booth Encoder is used by Partial Product Generator and uses these signals to choose from and extend signs of '0', MD or -MD for creating 8 partial products. The 8 partial products are given to Wallace Tree and then added appropriately. The Wallace tree uses both Full Adder and Half Adders. The final 16-bit intermediate results are added using a Carry Look-ahead Adder.

D. Carry Look-Ahead Adder

Function: Carry Look-ahead Adder (CLA) add two numbers with very lower delay.

Algorithm: By extend the cin with the corresponding inputs, the carry and sum are independent of the previous bits. (this carry look–ahead adder is implement as in the reference paper18 but by using ECRL and, or, xor, mux gates for ECRL partial product generator and by using EEAL and, or, xor, mux, gates for EEAL partial product generator).

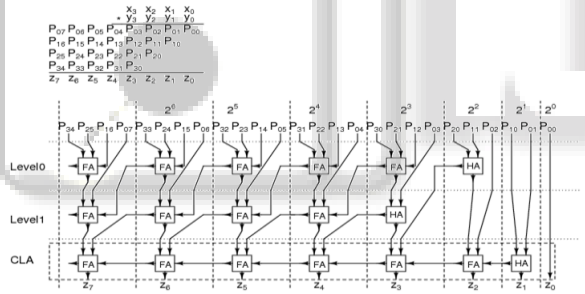

Fig. 2.8: Wallace tree Multiplier Architecture

E. Ecrl Partial Product Generator

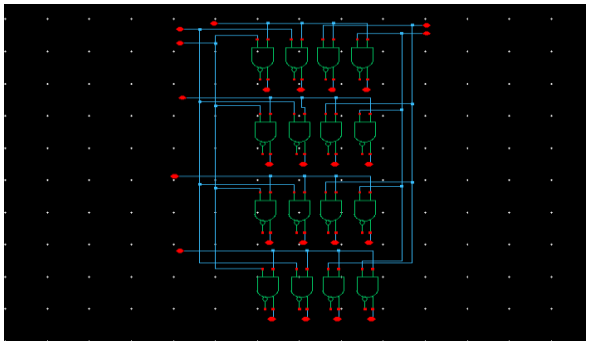

Fig. 2.9:

F. ECRL Wallace Tree Multiplier Architecture

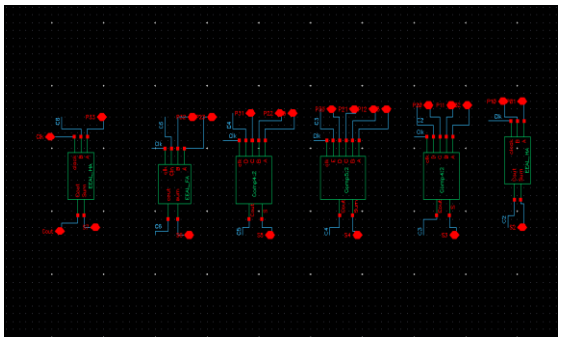

Fig. 2.10:

G. ECRL Adiabatic Multiplier

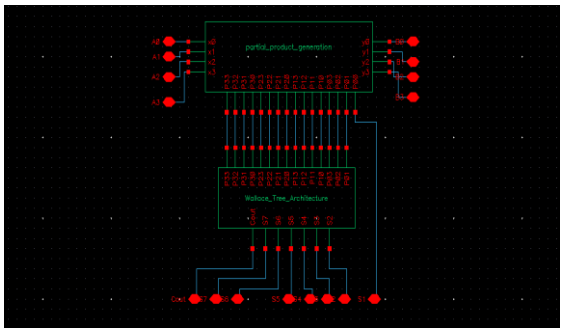

Fig. 2.11:

H. EEAL Adiabatic Multiplier

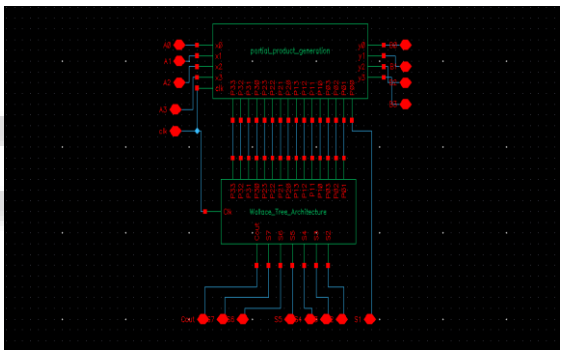

Fig. 2.12:

IV. FINFET BASED STATIC AND ADIABATIC LOGIC

Three basic working modes for FinFET, are 1)Short-Gate mode, 2)Independent-Gate mode 3)Low-Power mode. It provides more design flexibility due to multigate structure. The front-gate and the back-gate of FinFET are tied together or be controlled independently by different voltages.

Short-Gate (SG) mode, where the double gates are tied together which forms a three-terminal device. It is a replacement for MOSFET. It is a high performance mode. Due to strong gate control it offers better suppression for the SCEs and gate-dielectric leakage.

Independent-Gate (IG) mode, to form two independent gates the top part of the gate is removed. This acts as a four-terminal device. IG FinFET can work as two parallel transistors, by connecting the front-gate and back-gate to different inputs. This reduces the number of transistors and improves the flexibility.

Low-Power (LP) mode, to reduce the threshold leakage the back-gate is connected to a reverse-bias.

Therefore threshold leakage can be adjusted by adjusting the back gate voltage. This is a special case of IG mode.

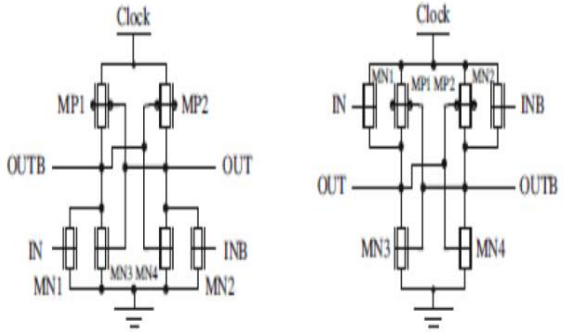

Fig. 2.13: Short Gated mode of Adiabatic Logic Gates

V. EXPERIMENTAL RESULTS

A. CMOS 180nm Static and Adiabatic gated 4x4 Wallace tree multiplier Parametric Analysis

4x4 Wallace Tree Multiplier	Average Current(Amps)	Average Delay(Secs)	Average Power(Watts)	Power Delay Product(Joules)
Static CMOS	22.6690u	7.4926n	71.2676u	533.9772f
ECRL	51.8809u	7.4581n	24.2917u	386.9345f
EEAL	16.9591u	2.5650n	28.3195u	72.6405f

Table 1.

B. Finfet 22nm Static And Adiabatic Gated 4x4 Wallace Tree Multiplier Parametric Analysis

4x4 Wallace Tree Multiplier	Average Current(Amps)	Average Delay(Secs)	Average Power(Watts)	Power Delay Product(Joules)
Static CMOS	5.6377u	7.3985n	4.4212u	32.7104f
ECRL	16.1258u	37.5983p	11.9923u	450.8898a
EEAL	7.2205u	29.1238p	4.2994u	125.2143a

Table 2.

Comparing the CMOS 180nm using Static and Adiabatic logic based 4x4 Wallace Tree multiplier and FinFET 22nm using Static and Adiabatic logic based 4x4 Wallace Tree multiplier we come to conclude FinFET based Architecture of Adiabatic Wallace Tree multiplier has much better performance over other static and CMOS based designs.

VI. CONCLUSION

In this work we design and analysis the 4x4 Wallace Tree Multiplier using Static and Adiabatic logic at CMOS 180nm and FinFET 22nm technology node. On our analysis we come to conclude our proposed Adiabatic Energy Efficient Adiabatic Logic based Wallace Tree 4x4 Multiplier architecture has higher speed (i.e. less delay) and Low power consumption one compared with other existing ECRL and Static Logic. So overall Figure-of-Merit of the proposed design is higher than other conventional designs. Moreover we designed and comparing the parametric performance characteristics on this 4x4 Wallace Tree multiplier architecture with CMOS 180nm and FINFET 22nm Scaled Process. Thus result shows that our proposed Energy Efficient Adiabatic logic based Wallace Tree multiplier architecture using FinFET 22nm design methodology has an enhanced performance and reliability over the Conventional design like ECRL and Static based designs.

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