A Novel Approach for Improving the Power Efficient and Meta stability Resistant Resilient Circuit

D.Maheswari[1] P.Nagarajan[2] C.M.Kalaiselvi[3] C.Dhivya[4]
[1,3,4]M.E Student [2]Assistant Professor
[1,2,3,4]Department of Electronics and Communication Engineering
[1,2,3,4]Vivekanandha college of engineering for women

Abstract— In this paper, a meta stability resistant caution flipflop (FF) is proposed, which consists of an edge detector, a caution window generator, and a caution detector along with a timing error resilient flip-flop. The delayed data are monitored during the caution window to flag a warning signal before the data enter the erroneous zone. In this scheme, the caution window is independent of input clock frequency and hence is suitable for frequency scaling application. The proposed flip-flop design routinely corrects timing errors and therefore minimizes the performance degradation due to variations.

Key words: Dynamic voltage scaling (DVS), Edge detector, Error Resilient Flipflop, Resilient circuits

I. INTRODUCTION

Conventional microprocessors require clock frequency (FCLK) guardbands to ensure correct functionality during worst-case dynamic operating variations in deliver voltage (VCC), temperature, and transistor aging. Consequently, these inflexible designs cannot use opportunities for higher performance by increasing FCLK or lower energy by reducing VCC during favorable operating conditions and be short of of aging degradation. Since most systems usually operate at nominal conditions where worst-case scenarios hardly ever occur, these infrequent dynamic constraint variations harshly limit the performance and energy efficiency of conservative microprocessor designs. This tutorial reviews a 65 nm resilient circuit test-chip is implemented with timing-error detection and revival circuits to eliminate the clock frequency guard band from dynamic supply voltage and temperature variation as well as to use path-activation probabilities for maximizing throughput.

One of the major challenges of employing DVFS technique is the variations in process, temperature and supply voltage that can significantly impact circuit functionality and performance especially at lower supply voltages. Several timing error detection and correction methods have been proposed in the literature.

Razor I flip-flop (FF) shows the way for the reduction of worst case margin [1]. It uses an error detecting FF on the critical trail of the design to decrease the supply voltage, which finds the first failure point for a given frequency. It allows the decrease in design margins most important to the significant energy saving. However, the technique requires additional circuitry, such as shadow latch and metastable detector for error recognition. The vital limitation of this technique is that it check the error at the yield of an FF, which requires a metastable detector to determine the yield of the FF. The canary FF uses a late data and a shadow FF along with the traditional FF to detect the timing error [2]. Since it compares the data at the output of an FF, it also requires metastable detector. Razor II is one more flavor of Razor I where data transition is checked at the input of an FF [3], [4]. Hence, it does not need a metastable detector. However, Razors I and II are used in a processor structure where the remedial action is performed using reexecution of instructions.

The proposed technique in this paper is a new metastability resistant warning FF, which is used in an ASIC framework [5]. The proposed circuit uses the idea of delayed data in the transition/edge detector, which flags the warning instead of the error. Since it reports the warning, the suitable data are captured correctly by the FF in the same clock cycle. In this paper, we propose a new flip-flop circuit with built-in timing-error detection and correction capability, called error resilient flip-flop (ERFF).

II. ERROR RESILIENT FLIP FLOP (ERFF)

Fig.1 shows the proposed timing error resilient flip-flop (ERFF) circuit, which is composed of four parts. The first two parts are similar to the master latch and the slave latch in traditional CMOS transmission-gate based D-type flip-flops. The third part is a 2-1 multiplexer, which bypasses the master latch if the input signal "D" transition occurs after the rising clock "CLK" edge. The last part is the late detector, which consists of a transmission-gate based XOR and a dynamic logic circuit. When there exists a signal change in D after the CLK goes high, the "Late" signal will be asserted and will remain asserted until CLK goes low. This causes D to bypass the master latch of ERFF. As a result, the ERFF output signal "Q" will simply follow its input D for the remaining positive CLK cycle.

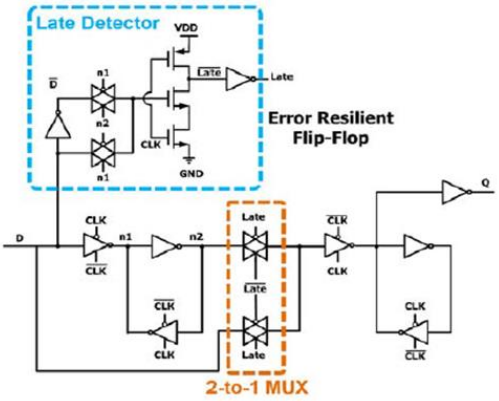


Fig. 1: proposed error resilient flip-flop (erff) circuit diagram.

III. CONCEPT OF WARNING DETECTION

Setup time: It is the time before the clock edge during which the data should be obtainable such that the data can be sampled correctly by the FF. The most horrible case setup time is the most horrible value of the setup time after performing statistically meaningful simulations (e.g., Monte Carlo) allowing for variation to the process parameters, such

as the gate length and the threshold voltage, and environmental parameters, such as the supply voltage and the temperature. The worst case setup time is denoted as twsetup.

Hold time: It is the time after the clock edge during which the data should be obtainable such that the data can be sampled correctly by the FF. The worst case hold time is found out next the method explained in the definition of worst case setup time. The worst case hold time is denoted as twhold.

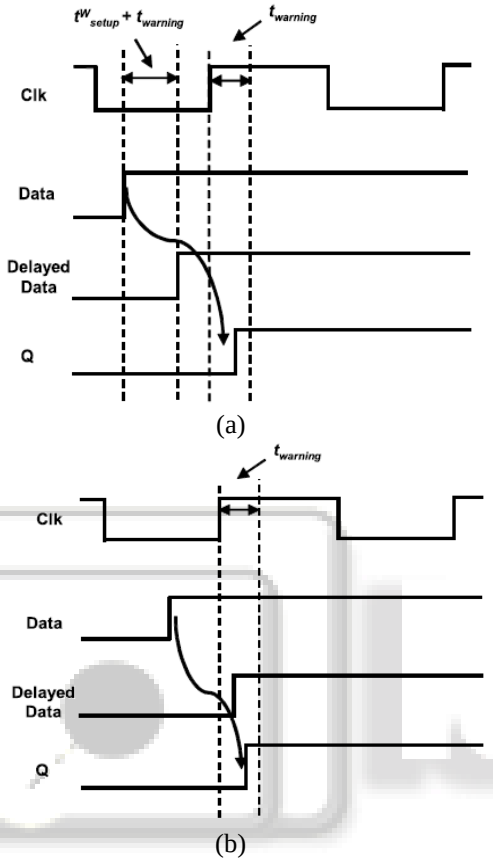


Fig. 2: Proposed warning detection using the delayed data showing the warning window after rising edge of the clock. (a) Early data arrival. (b) Late data arrival.

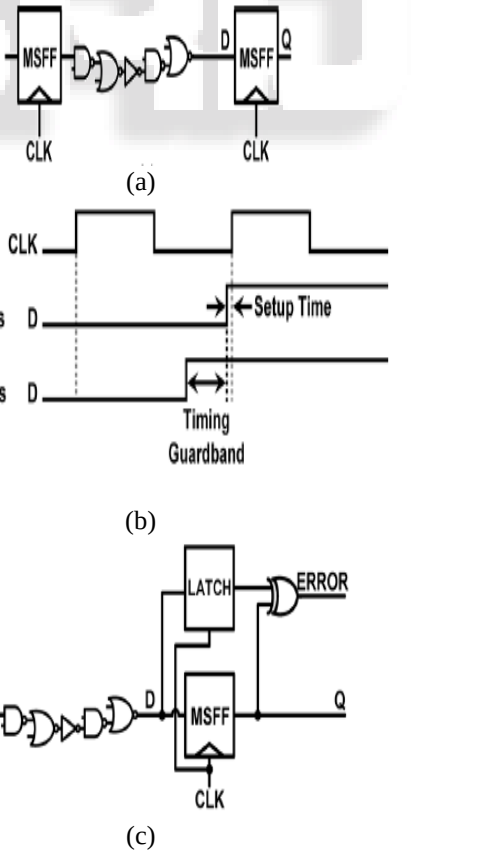
In our warning detection scheme, the warning is detected by monitoring the delayed data transition. In case of the delayed data, the warning window twarning is after the rising edge of the clock, as shown in Fig. 1(a). The minimum delay bound between delayed and direct data is equal to the sum of twsetup and twarning , as shown in Fig. 1(a), so that the warning window will appear after the rising edge of the clock. The same amount of delay between direct and delayed data is maintained in both Fig. 1(a) and (b). However, delayed amount is only shown in Fig. 1(a) and not shown in Fig. 1(b) to maintain the clarity of the figure. When the data arrive early, both the data and delayed data are outside the warning window, as shown in Fig. 1(a). When the data arrive late, the data are outside the warning window and the delayed data are inside the warning window, as shown in Fig. 1(b). Since, the delayed data are inside the warning window, the data are safely sampled by the FF in the rising edge of the clock, as shown in Fig. 1(b). The corrective action should be taken after multiple clock periods such that the delayed data transition would not happen in the warning window. In this paper, the delayed data transition is monitored in the warning window to flag warning signal.

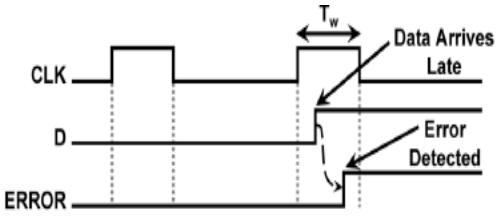
IV. PROPOSED SYSTEM

The circuit consists of an edge detector, a warning window generator, and a warning detector subcircuits along with a Error resilient circuit, as shown in Fig. 2. The timing error can be monitored by two methods, such as: 1) monitoring input data transition during the warning window and 2) comparing the output of a FF with that of another FF. The latter method requires metastable detector to resolve the time critical data. However, in this paper, the data transition at the input of the FF is monitored to prevent the timing error. The proposed approach two error-detection sequential (EDS) circuits are introduced to preserve the timing-error detection capability of previous EDS designs while lowering clock energy and removing datapath metastability. One EDS circuit is a dynamic transition detector with a time-borrowing datapath latch (TDTB). The other EDS circuit is a double-sampling static design with a time-borrowing datapath latch (DSTB). Error-recovery circuits are introduced to replay failing instructions at lower clock frequency to guarantee correct functionality.

A. Eds Circuit Overview:

The basic idea of timing-error detection circuits for dynamic variation tolerance is described in Fig. 2. A conventional path with master-slave flip-flops (MSFF) is provided in Fig. 2(a) along with conceptual timing diagrams in Fig. 2(b), illustrating the arrival times of the input data (D) to the receiving flip-flop during worst-case dynamic variations and nominal conditions



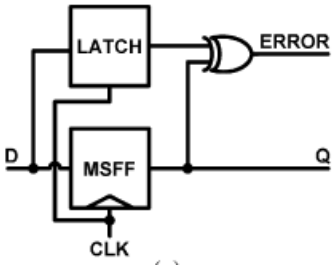


(d)

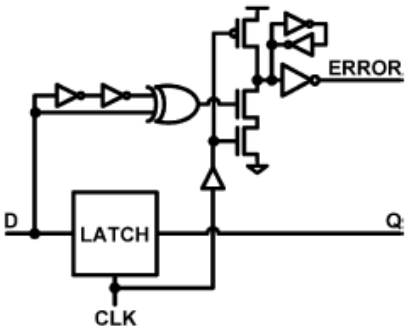
Fig. 3 (a) Conventional path design with (b) conceptual timing diagrams for worst-case dynamic variations and nominal conditions. (c) Resilient path design [5]–[9] with (d) conceptual timing diagram for late arriving input data.

Within the presence of worst-case dynamic variations, the input data to the receiving flip-flop must arrive a setup time prior to the rising clock edge to ensure correct functionality. In comparison, the input data for the same path arrives much previous during nominal conditions.

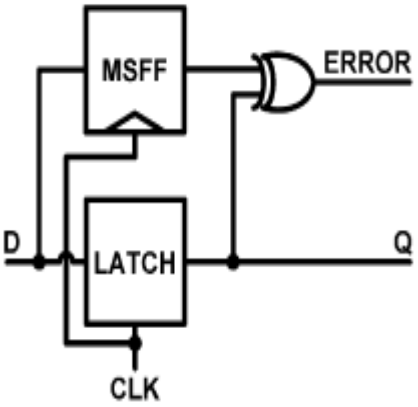
The difference between the input data arrival times for these two cases represents the effective timing guardband required for dynamic variations. A resilient path is created by replacing the receiving MSFF of the conventional path with an EDS circuit as described in Fig. 2(c). The conceptual timing diagram in Fig. 2(d) illustrates late arriving input data. The EDS circuit in Fig. 2(c) and Fig. 3(a) is a simplified Razor flip-flop (RFF) [6]–[7], where the metastability detector is omitted. The (RFF) [6]–[7], where the metastability detector is omitted. The RFF double samples input data with a datapath flip-flop on the rising clock edge and a shadow latch on the falling clock edge. The flip-flop and latch outputs are compared with an XOR gate to produce an error signal (ERROR). If input data transitions late as described in Fig. 2(d), flip-flop and latch outputs differ, resulting in a logic-high error signal. The error signal is handled at the microarchitecture level to enable error recovery. Since the resilient circuit can detect and correct late arriving data, the timing guardband for dynamic variations in the conventional design can be removed, allowing the resilient circuit to operate at a higher FCLK.



(a)



(b)



(c)

Fig. 4: Error-detection sequential circuits: (a) Razor flip-flop (RFF), (b) transition detector with time borrowing (TDTB), and (c) double sampling with time borrowing (DSTB). CLK is duty-cycle controlled to satisfy min-delay requirements.

B. Edge Detector:

Normal edge detectors use either static CMOS logic style [8] or dynamic logic style [9]. However, the proposed edge detector is a pass-transistor-based design, as shown in Fig. 4, The proposed edge detector consists of two inverters I1 and I2 ,a conditional inverter I3 , and a transmission gate T ,as shown in Fig. 4. In this approach, the output of the conditional inverter I3 and the output of the transmission gate T are connected to generate the output of the edge detector. When delayed data = 1, the conditional inverter I3 behaves as a normal inverter and its output acts as the output of the edge detector. In this case, transmission gate T is not operational. When delayed data = 0, the transmission gate T is operational and its output acts as the output of the edge detector. In this case, the conditional inverter I3 is not operational. The control signals (i.e., outputs of I1 and I2) for the transmission gate T and inverter I3 are same, which allows either inverter I3 or transmission gate T to be active at one time. The input signal (i.e., delayed data) for transmission gate T and inverter I3 are same. However, the delays of inverter I and transmission gate T are not same. Hence, there would be small amount of race due to the delay difference between inverter I transmission gate T.

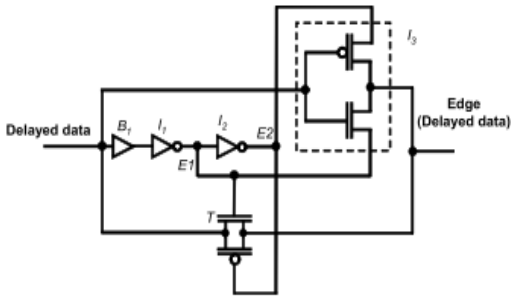


Fig. 5: Pass-transistor-based edge detector.

C. Warning Window Generator:

The warning window is also known as guard band interval in [10], time window control (TWC) in [11], and detection window in [12]. The creation of the warning window is explained in the following two cases.

1) Case I—Before the Rising Clock Edge: The guard band interval in [10] and the TWC in [11] are created before the rising clock edge of a positive edge triggered FF. In

this approach, the warning window is generated for a rising edge from the previous rising edge. Accordingly, the previous rising edge acts as the reference signal for generating warning window for the present rising edge. In this case, the warning window width depends on clock frequency and designed for a fixed clock frequency. It requires a large number of buffers to create the required warning window before the rising clock edge, which in turn leads to increase in area and power dissipation in low clock frequency. However, the edge detector in this approach operates with input data directly. The detection window in [12] is generated from the leaf clock by inserting buffer cells in the path, which leads to huge dynamic power consumption. In this approach [12], the clock for the FF also has delay cells so that the detection window is created before the rising clock edge for the FF, which creates difficulty in balanced clock tree synthesis.

2) Case II—After the Rising Clock Edge: In our approach, the warning window is generated after the rising edge of a positive edge triggered FF. In this case, the warning window is generated for a rising edge from the same rising edge. Accordingly, the same rising edge acts as the reference signal for creating the warning window. Hence, it would require a few buffer chains. In this case, the warning window width is independent of clock frequency. A few buffer chains in the clock path make the warning window generator circuit area and power efficient. The warning window is generated by logical AND operation between the clock signal and the delayed inverted clock signal, as shown in Fig. 5. In this case, the edge detector operates with the delayed data. The width of the warning window is determined by the buffer inserted in the inverted clock path, as shown in Fig. 5.

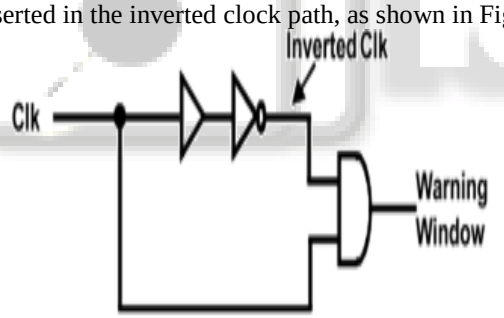


Fig. 6: Circuit for generating warning window from clock signal

D. *Delay Buffer And Warning Detector:*

The delay buffer used in the warning FF is basically a chain of buffers. Let tw setup is the worst case setup time considering the process, voltage, temperature variation, and clock skew and jitter and tmin warning is the minimum width of the warning window considering worst case process, supply, and temperature variation. Then, the minimum delay of the buffer tminbuffer is given by

Tmin buffer ≥ tw setup + tminwarning.

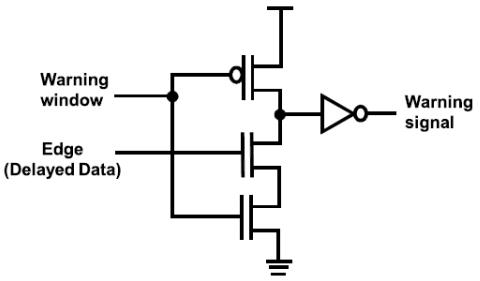


Fig. 7: Circuit for Delay buffer

V. SIMULATION RESULTS

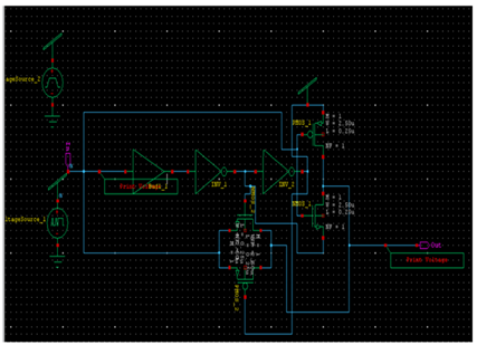


Fig. 8: Schematic view of edge detector circuit

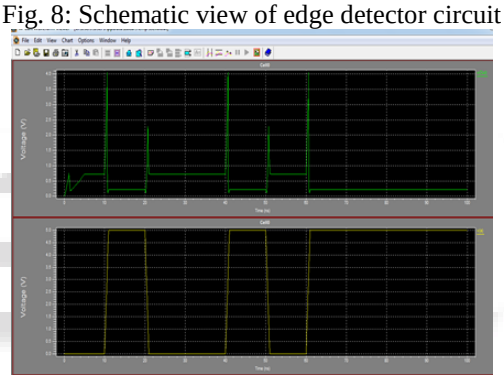


Fig. 9: Edge detector output waveform

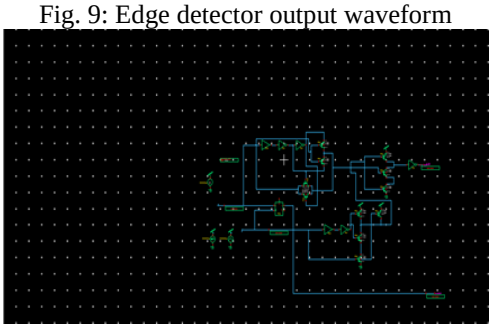


Fig. 10: Schematic view of warning FF

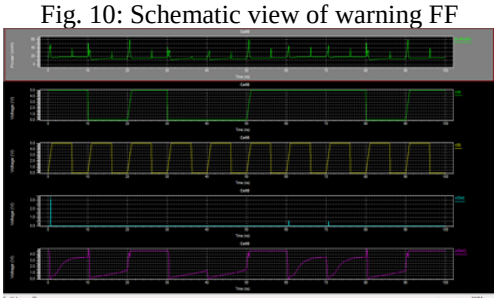


Fig. 11: Warning FF output waveform

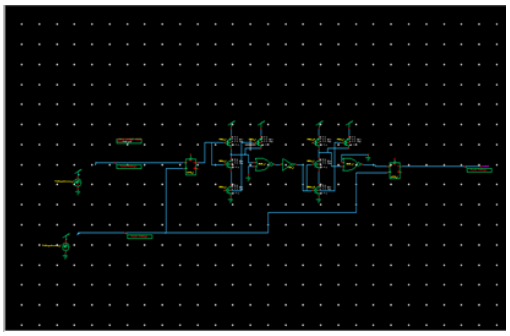


Fig. 12: Schematic view of Resilient circuit

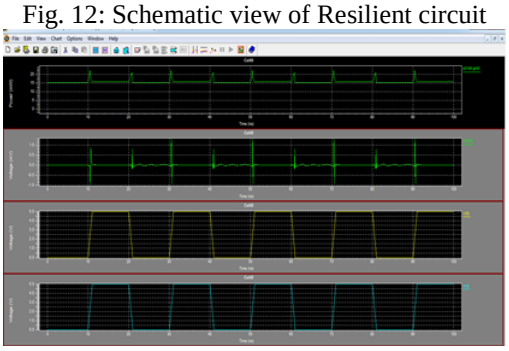


Fig.13: Output of Resilient circuit

Table.1 Shows the average power consumed by warning FF and Resilient circuit

BLOCK DESIGN	AVERAGE POWER CONSUMPTION
EDGE DETECTOR	3.524768e-002 watts
WARNING FF	1.683870e-002 watts
RESILIENT CIRCUIT	1.574171e-002 watts

Table 1: Average power comparison table

VI. CONCLUSION

This paper proposes a metastability resistant caution detection sequential using the idea of delayed data in the edge detection circuit and a resilient circuit. Timing-error detection and recovery circuits are implemented in a resilient circuit test-chip to remove the clock frequency FCLK guard band from dynamic supply voltage VCC and temperature variation as well as to exploit path-activation probabilities for maximizing throughput.

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