

A Novel Design of 3-Bit Gray Code Counter Using Reversible Logic Gates

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Abstract— The Reversible logic synthesis technique is most important part of the long-term future of computing due to its low power dissipating characteristic. In recent years, reversible logic circuits have attracted considerable attention in improving some fields like nanotechnology, quantum computing, cryptography, optical computing and low power design of circuits due to its low power dissipating characteristic. In this paper we proposed the design of 3-bit Gray Code counter which uses reversible gates and derived quantum cost, constant inputs, garbage output and number of gates to implement it.

Key words: Reversible logic gate, Counter, Constant input, Garbage output, Delay

I. INTRODUCTION

Landauer states that the loss of one bit of information dissipates $KT \ln 2$ joules of energy, where K is the Boltzmann constant and T is the absolute temperature at which the operation is performed [1]. At room temperature the heat dissipation due to loss of one bit of information is very small but not negligible. This computation procedure is irreversible. Further Bennett, showed that one can avoid $KT \ln 2$ joules of energy dissipation from the circuit if input can be extracted from output and it would be possible if and only if reversible gates are used [2]. Research is going on in the field of reversible logic and a good amount of research work has been carried out in the area of reversible combinational logic. However, there is not much work in the area of sequential circuit like flip-flops and counters. A counter, by function, is a sequential circuit consisting a set of flip-flops connected in a suitable manner to count the sequence of the input pulses presented to it in digital form [10]. In Synchronous counters the flip-flops are clocked at the same time by a common clock pulse. This paper proposes a novel design of 3-bit Gray Code counter using reversible logic gates.

II. BASIC CONCEPTS

This section explains some basic concepts of reversible gates and quantum circuits which are as follows:

A. Reversible Logic Function

It is an n -input n -output logic function in which there is a one-to-one correspondence between the inputs and the outputs, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs. [6] This prevents the loss of information which is the root cause of power dissipation in irreversible logic circuits. Energy dissipation can be reduced or even eliminated if computation becomes Information-lossless. The reversible logic circuits must be constructed under two main constraints. They are:

- Fan-out is not permitted.
- Loops or feedbacks are not permitted

Quantum logic gates have some properties as shown in “(1.1).”

$$\left. \begin{aligned} V \times V &= NOT \\ V \times V^+ &= V^+ \times V = I \\ V^+ \times V^+ &= NOT \end{aligned} \right\} (1.1)$$

Any reversible logic gate (circuit) is realized by using mentioned gates above, NOT and FG gates. The properties above show that when two V gates are in series they will behave as a NOT gate. Similarly, two V^+ gates in series also function as a NOT gate. A V gate in series with V^+ gate, and vice versa, is an identity.

B. Garbage Output

This refers to the number of unused outputs present in a reversible logic. A garbage output is an output that is needed to change an irreversible gate to a reversible one and are not used to the input to the other gates

C. Quantum Gate

Quantum gates are reversible and based on quantum computing. For realizing 1×1 and 2×2 quantum gates we can use quantum technique. Since bigger quantum gates like 3×3 , 4×4 etc. cannot be realized by quantum technique directly, 1×1 and 2×2 quantum gates are used for realizing this bigger quantum gates.

D. Quantum Cost

This refers to the cost of the circuit in terms of the cost of a primitive gate. The quantum cost of a reversible gate is the number of 1×1 and 2×2 reversible gates or quantum gates required in its design. The quantum costs of all reversible 1×1 and 2×2 gates are taken as unity. Since every reversible gate is a combination of 1×1 or 2×2 quantum gate, so the quantum cost of a reversible gate can be calculated by counting the numbers of NOT, Controlled- V , Controlled- V^+ and CNOT gates used. [3], [14]

E. Reversible Gate

A gate with equal number of input and output in which input and output have one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. If the input vector of a reversible gate is denoted by $I_V = (I_1, I_2, I_3, \dots, I_K)$, the output vector can be represented as $O_V = (O_1, O_2, O_3, \dots, O_K)$. A reversible gate can be represented as $K \times K$ in which the number of input and output is K .

F. Feynman Gate (cnot gate)

The Feynman gate (FG) or the Controlled-NOT gate (CNOT) is a 2-input 2-output reversible gate having the mapping (A, B) to $(P = A, Q = A \oplus B)$ where A, B are the inputs and P, Q are the outputs, respectively. [5]. Since it is a 2×2 gate, it has a quantum cost of 1. “Fig. 1” and “Fig. 2” shows the block diagram and quantum representation of the Feynman gate. “Fig. 3” and “Fig. 4” shows the block diagram and quantum representation of Double Feynman

Gate respectively. Quantum cost of DFG is 2 as it needs two CNOT gate to implement it.

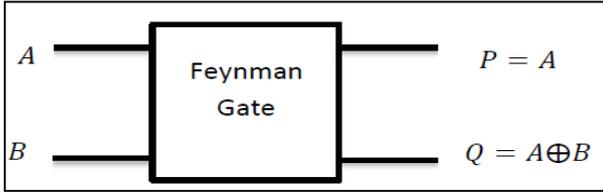


Fig. 1: 2X2 Feynman

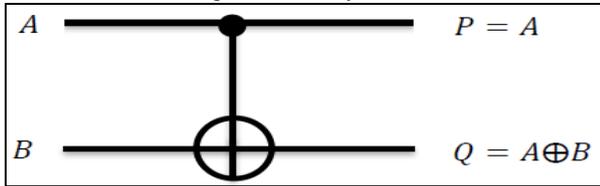


Fig. 2: Quantum representation of Feynman

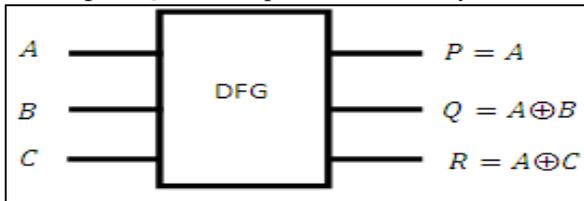


Fig. 3: Double Feynman Gate

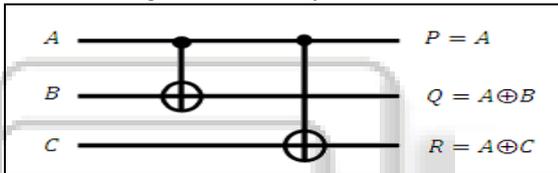


Fig. 4: Quantum Representation of DFG

G. SAM Gate

Input vector I_v and Output vector O_v are represented as $I_v=(A,B,C)$ and $O_v= P = \bar{A}, Q = \bar{A}B \oplus A\bar{C}, R = \bar{A}C \oplus AB$ and respectively. The block diagram of 3x3 SAM gate is shown in “Fig. 5” and its quantum representation is shown in “Fig. 6”. The quantum cost of SAM gate is 4. [4],[9]

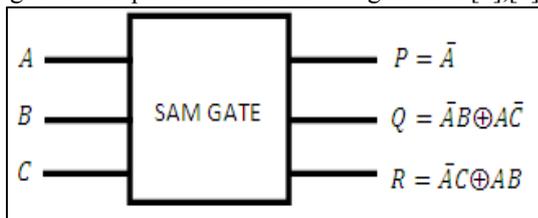


Fig. 5: Block diagram of 3x3 SAM Gate

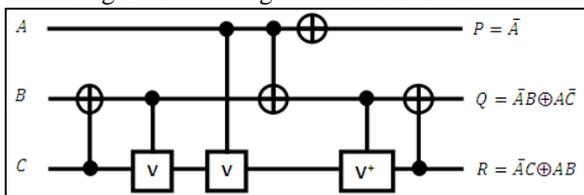


Fig. 6: Quantum representation of SAM gate.

If we give 0 to 3rd input then we get NOT of 1st input in 1st output, OR of 1st and 2nd inputs in 2nd output and AND of 1st and 2nd inputs in 3rd output. This operation is

shown in “Fig. 7”. So this gate can be used as two input universal gate.

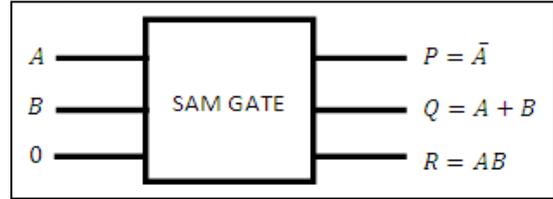


Fig. 7: SAM as NOT, OR and AND.

The Characteristic equation of D Flip-Flop is $Q = \overline{CLK}.Q + CLK.D$ “Fig. 8” shows the D flip-flop implementation by using SAM and DFG gate. Quantum cost of this D Flip-Flop implementation is 6.[7]-[8][11]-[13]

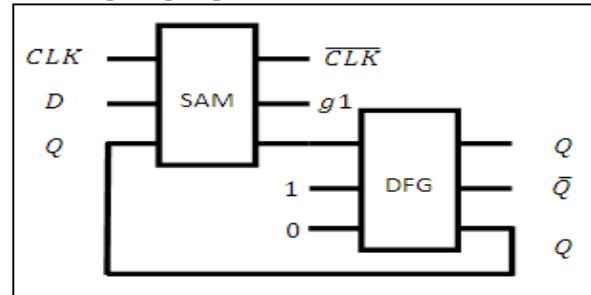


Fig. 8: D Flip-Flop

III. PROPOSED WORK

A. 3-Bit Gray Code Counter

The 3-bit Gray Code counter is constructed by D flip-flop. The truth table given in Table-I, one can observe that, for a 3-bit Gray Code counter, there are 8-states.

| Present State | | | Next state | | | Flip-Flop Input | | |
|----------------|----------------|----------------|----------------|----------------|----------------|-----------------|----------------|----------------|
| q ₂ | q ₁ | q ₀ | Q ₂ | Q ₁ | Q ₀ | D ₂ | D ₁ | D ₀ |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |

Table 1: Truth table of 3-bit Gray Code counter

B. Flip-Flop Input Equations

After Solving with the help of K-map, we get the Equations as given below:

$$D_2 = Q_1 \cdot Q_0' \oplus Q_2 \cdot Q_0$$

$$D_1 = Q_1 \cdot Q_0' \oplus Q_2' \cdot Q_0$$

$$D_0 = (Q_1 \oplus Q_2)'$$

C. Proposed Design of 3-bit Gray Code Counter

“Fig. 9” shows the proposed design of 3-bit Gray Code counter using SAM, FG and DFG gates

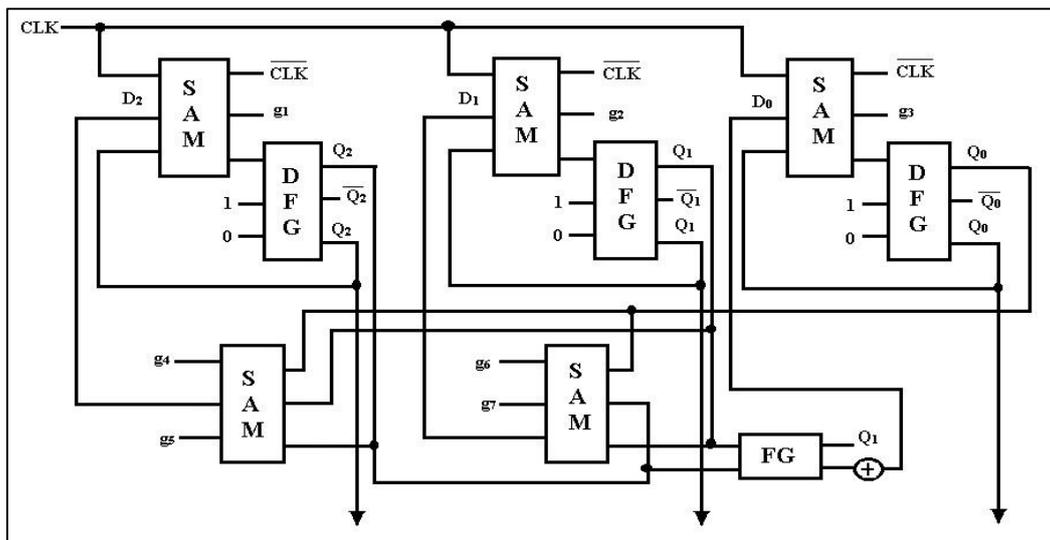


Fig. 9: Proposed Design of 3-bit Gray Code Counter.

IV. RESULTS AND DISCUSSION

In the implementation of 3-bit Gray Code counter we use Five SAM gate having Quantum cost (QC) of 4 and three DFG gate having Quantum cost =2 and one FG having QC of 1. Number of gates, constant inputs, garbage output and quantum cost are shown in Table-II.

| No of Gates | No. of constant input | No. of garbage output | Quantum cost |
|-------------|-----------------------|-----------------------|--------------|
| 9 | 6 | 8 | 27 |

Table 2:

V. CONCLUSION

We have presented the basic concepts of multipurpose binary reversible gates. Such gates can be used in regular circuits realizing Boolean functions. This paper proposes designs of basic reversible sequential elements such as flip-flops and 3-bit Gray Code counter. In this paper, we implement a 3-bit Gray Code counter design directly from reversible gates. Minimization of Quantum cost, garbage output and number of gate is a challenging one. Here in this paper the proposed designs are better in terms of quantum cost and garbage outputs. The proposed design can have great impact in quantum computing. The proposed synchronous counter designs have the applications in building reversible ALU, nanotechnology, low power circuit design, cryptography, optical computing etc.

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