Implementation of Efficient Full Adder using MVL Technique

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Abstract— The digital logic circuits are restricted for the requirement of interconnections. This difficulty overcomes by using a big set of signals over the same chip area. Multiple-valued logic (MVL) designs contain more importance from that perspective. This paper gives the fabrication of a multiple-valued half adder and full adder circuits. This technique advantageous for large scale circuits due to which large power dissipation with increased speed can lead to the development of extremely low energy circuit's use for the high performance required for number of applications. Multiple-valued logic (MVL) designs are gaining more advantageous from the design of a multiple-valued half adder and full adder circuits. The presented adders are design in Multiple-Valued voltage-Mode Logic (MV-VML). In quaternary half adder, quaternary logic levels are exploited for the intention of addition. Addition operation is executed with minimum number of gates and less depth of net. The design is targeted for the 0.18 µm CMOS technology. Circuit is design by using Advanced Design System software {ADS software}. In this paper we try to find area, power and speed of the design HAq / FAq without any need of conversion, and compare to existing binary circuits [HAb / FAb].

Key words: MVL, Full Adder

I. INTRODUCTION

Multiple value logic is logical calculi which contain more than two possible truth values. Logical calculi are bivalent. There are only two possible values for any proposition true and (1's or 0's) that is in the form of. Lukasiewiczs was first author who present two value and three value logic. i.e (True, false and unknown). Today's four value logic which we called quaternary logic concept is applied. Increased data density, optimize dynamic power dissipation, and increased computational ability are among some of the key benefits of Multiple Valued Logic (MVL). Number of implementation methods has been proposed in the latest papers to realize the MVL circuits [6]. They can fundamentally classified as current-mode, voltage-mode and mixed-mode circuits current-mode circuits [3, 8] have been popular and offer several benefits, the power consumption is high due to their inherent nature of constant current flow during the operation.

Alternatively, voltage-mode circuits exhaust a large majority of power only during the logic level switching. Hence, voltage-mode circuits provide lesser power consumption which has been the key advantage of traditional CMOS binary logic circuits from the perspective of dynamic switching procedure. Several approaches for quaternary circuit design have been proposed [7 - 9], in voltage mode technique. Quaternary logic (radix-4-valued) is chosen as the base radix for the work reported here. Using a quaternary radix offers all the advantage of MVL such as minimization of area due to signal routing reduction along with the important benefits of being able to easily interface with traditional binary logic circuits.

Multiple PLC technologies to be bridged to form very large networks. Generally power networks can be classified into three broad categories: dc current supply used in industrial applications such as automotive; sinusoidal supply used for electrical distribution networks or domestic applications; and pulse width-modulated (PWM) networks used in the vast majority of applications involving converters and actuators. Power-line communication (PLC) technology is widely used over sinusoidal and continuous electrical networks and data rates up to several hundred megabits per second are guaranteed. Those PLC modems cannot operate on PWM networks who present, by nature, a broad spectral occupancy. Thus, this seminar proposes an overview of the PLC technology and its operating limits over a PWM network. Based on a detailed study of the inverter spectrum, new PLC modems dedicated for the PWM network are developed. The capacity of these modems in terms of transmission reliability and data rate is evaluated. This technology avoids using any additional cables between the actuator and the converter which can be advantageous in terms of price and overall dimension.

II. LITERATURE REVIEW

A. *Vasundara Patel, K S Gurumurthy*

"Arithmetic operations in multi-valued logic", International journal of VLSI design and communication system (VLSICS), vol.1, no.1, pp. 21-32, March 2010.

1) Theory Details:

Author presents arithmetic operations like addition, subtraction and multiplications in Modulo-4 arithmetic, and also addition, multiplication in Galois field, using multi-valued logic (MVL). Author use hspice as tool for simulation, and Q-B conversion, B-Q conversion for implementation the arithmetic operation, for minimization of logic Karnaugh diagrams being used.

2) Our Finding:

From this paper we find that, Circuits for Modulo-4 addition, multiplication and subtraction require only 4 gates. Galois addition requires two xor gates which is most optimized one among other circuits while implementing in VLSI. With the help of quaternary logic levels, they have reduced the interconnections.

B. *Bob Radanovic, Marek Syrzycki*

"Current-Mode CMOS Adders Using Multiple-Valued Logic", Canadian Conference on Electrical and Computer Engineering, pp.190-193, 1996.

1) Theory Details:

They presents the adder cell for radix 2 algorithm, using PD(Positive Digit) representation , they use two technology 0.8um cmos and 1.5um cmos , with step current of 12uA and 1uA respectively. They Also address the design of 4 digit decimal adder with 10 step of current.

2) Our Finding:

Two major issues in efficient design of CMMV circuits are the numerical representation of numbers and the unit current

step per logic level. A (PD) represent positive currents to encode the numbers, but increased circuit complexity. Proper choice of multiple value algorithm and current levels can potentially result in very high speed operation and low power supply which is very attractive in VLSI chip.

C. Ricardo Cunha, Henri Boudinov and Luigi Carro

"Quaternary Look-up Tables Using Voltage-Mode CMOS Logic Design", ISMVL 2007, 37th International Symposium on Multiple-Valued Logic, pp.56-56,13-16 May, 2007.

1) Theory Details:

Presented a new way to implement quaternary look-up tables using a multiplexer circuit to implement any quaternary logic function based on its truth table. Result has been compare with binary. Simulation has been carried out in Spice tool using TSMC 0.18 µm.

2) Our Finding:

We find that by using voltage mode cmos logic design in quaternary look up table is gives high performance with negligible static and dynamic power consumption with less power dissipation and less no. of transistor as compared to current mode CM MVL. But circuit complexity increases due to multiplexer.

D. Hirokatsu Shirahama and Takahiro Hanyu

"Design of High-Performance Quaternary Adders Based on Output-Generator Sharing", Proceedings of the 38th International Symposium on Multiple Valued Logic, pp. 8-13. 2008.

1) Theory Details:

Present Simple implementations of quaternary full adders are proposed for a high-performance multi-processor which consists of many processing elements (PEs). Result shows the delay of the proposed CM implementation is reduced to 70% and the delay and power dissipation of the proposed VM implementation are reduced to 73% and 79%, respectively

2) Our Finding:

The use of appropriate input-value conversion makes it possible to reduce the number of output generators, which enables to implement high performance quaternary full adders.

E. Anindya Das1, Ifat Jahangir2 and Masud Hasan

"Design of Quaternary Serial and Parallel Adders", 6th International Conference on Electrical and Computer Engineering ICECE 2010, 18-20 December 2010, Dhaka, Bangladesh.

1) Theory Detail:

Author presents/implement the design of a logarithmic stage parallel adder which can compute the carries within log2(n) time delay for n value computing. Author compares the gate delays of full adder and logarithmic stage parallel using mathematical expressions.

2) Our Finding:

Linearly increasing gate delay is the main disadvantage of ripple carry adder. So they have proposed logarithmic stage carry look-ahead adder which works within log2(n) gate-delay for n qudits and have limited number of fan-in.

F. Yasuda, Y. Tokuda, S. Zhaima, K. Pak, T. Nakamura A. Yoshida

"Realization of quaternary logic circuits by n-channel mos devices", IEEE Journal of Solid State Circuits, vol.21, no.1, pp.162-168, 1986.

1) Theory Details:

Author presents / implement the new method for quaternary circuits using NMOS devices is proposed. Several fundamental circuits such as inverter, NAND, NOR, and delta literal have been fabricated by conventional NMOS technology. These circuits are comprised of MOS transistors with three values of enhancement-mode threshold voltage and one depletion-mode threshold voltage.

2) Our Finding:

The new method to implement quaternary circuits using NMOS devices is proposed. Several fundamental circuits such as inverter, NAND, NOR, and delta literal have been fabricated by conventional NMOS technology. These circuits are comprised of MOS transistors with three values of enhancement-mode threshold voltage and one depletion-mode threshold voltage.

G. Jean-Marc Philippe, S´ebastien Pillement, Olivier Sentieys

"A low-power and high-speed quaternary interconnection link using efficient converters",

1) Theory Detail:

They introduce a new quaternary link including a binary-to-quaternary encoder and a quaternary-to-binary decoder in voltage mode multiple-valued logic (MVL). This link improves the transistor count compared to existing designs and it has no DC current path.

2) Our Finding:

This approach can increase the bandwidth of a link or can enable the designer to save silicon area. It has up to 46% less power consumption than a full-swing signalling system for long global interconnects. This link is also adapted to design high-speed interconnects due to its low propagation delay.

III. PROPOSED WORK

In this paper we will propose the quaternary half adder and full adder by using quaternary input and will obtained the quaternary output without using any converter. No need to convert the quaternary input into binary or binary to quaternary. From this method we can minimize the h/w implementation, power dissipation of circuit, require less number of transistor and we will achieve the high performance.

A. Implementation of Quaternary / Mvl for Half Adder

In quaternary logic, addition can be performed in many ways. Numbers in quaternary logic can be directly added or numbers in quaternary logic can be converted to binary logic and addition can be performed in binary logic. Binary results of addition can be displayed in quaternary logic after conversion. But we will perform the addition only by using quaternary logic only. In [10] modulo-4 addition is introduced, implementation of carry without hardware. Figure 1 explains the block diagram of quaternary half adder and table. An and Bn are quaternary input numbers and Sn and Cn are the quaternary output numbers.

Fig. 1: Block diagram of Quaternary half adder.

A_q	B_q	S_q	C_q
0	0	0	0
0	1	1	0
0	2	2	0
0	3	3	0
1	0	1	0
1	1	2	0
1	2	3	0
1	3	0	1
2	0	2	0
2	1	3	0
2	2	0	1
2	3	1	1
3	0	3	0
3	1	0	1
3	2	1	1
3	3	2	1

Table 1: Truth Table of Quaternary Half Adder.

B. Implementation of Quaternary Full Adder

Proposed full adder circuit is based on Quaternary adder. Block diagram of the full adder circuit is shown in figure 1. Logic levels of quaternary inputs 0, 1, 2 and 3 are represented by the voltage levels of 0V, 1V, 2V and 3V respectively. X and Y are the two quaternary inputs to the full adder. Table 1 shows sum and carry for all possible combinations of inputs when carry input is zero. Table 2 shows sum and carry for all possible combinations of inputs when carry input is one. An, Bn and Cn are quaternary input numbers and Sn and Cn are the quaternary output numbers.

	An					**An**				
Bn		0	1	2	3		0	1	2	3
	0	0	1	2	3	0	0	0	0	0
	1	1	2	3	0	1	0	0	0	1
	2	2	3	0	1	2	0	0	1	1
	3	3	0	1	2	3	0	1	1	1

Table 1: Truth tables of quaternary full addition, when carry in is 0

	An					**An**				
Bn		0	1	2	3		0	1	2	3
	0	0	1	2	3	0	0	0	0	0
	1	1	2	3	0	1	0	0	0	1
	2	2	3	0	1	2	0	0	1	1
	3	3	0	1	2	3	0	1	1	1

Table 2: Truth tables of quaternary full addition, when carry in is 1

Fig. 2: Proposed Quaternary Full Adder.

IV. CONCLUSION

In this paper we review the historical developments in this field, both in circuit realizations and in methods of handling multiple-valued design circuit. In the recent years MVL gaining the importance due to its inherent benefits like high speed, low area, and low power(Vm), we found during analysis of MVL, it has great high message communication ability. in earlier work quaternary [mvl0-3] arithmetic operations like addition, subtraction and multiplications presented which use q-b conversion, b-q conversion for implement the arithmetic operation. We proposed half adder and full adder in quaternary to quaternary without any conversion which then lead more optimization at farther level.

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