

Optimizing the Performance of Adders using Multiplexer and NAND Gates

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Abstract—In This paper provides the performances of adder’s circuit is proposed. The adder circuit is a very familiar method for optimizing speed, surface area. The area, speed is also important parameter to determine the performance of the system. In this paper, the full adder and half adder circuit cells are converting MUX and NAND gates. This type of adders used for design of field programmable gate arrays (FPGA). Simulations can be done by Xilinx 13.1i and layouts for MICROWIND EDA tool with supply voltage 1.8v.

Key words: MUX, NAND, FPGA, MICROWIND EDA, Xilinx

table is given as
 $S=A'B+AB'$
 $C=AB$

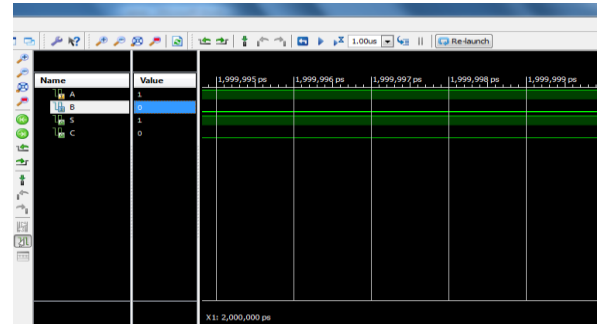


Fig. 2 simulation result of half adder on ISE Design Suite

I. INTRODUCTION

We are implementing new adders that adders are constructing with MUX and NAND gates. In most of these systems, the adder is part of the critical path that determines the overall performance of the system and the full adder is the core element of complex arithmetic circuits. That is why enhancing the performance of the 1-bit full-adder and half adder cell (the building block of the binary adder) is considered a significant goal.

The Full Adder and half adder is proven to use MUX construction have the minimum area and less delay product by simulation using Xilinx ISE 13.2i and schematic is proven by micro wind DSCH tool. A multiplexer is a combination of logic gates resulting into circuits with two or more inputs (data inputs) and one output. When compared to NAND gates MUX is faster and less time consuming.

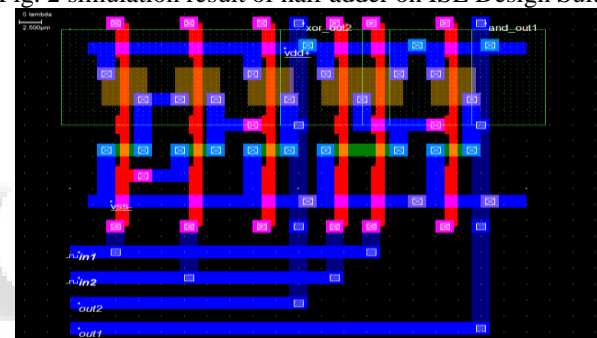


Fig. 3: Full automatic layout design of half adder

II. HALF ADDER DESIGN

Half adder circuit needs two binary inputs and two binary outputs. The input variables designated the augends and added bits; the output variables produce the sum and carry.

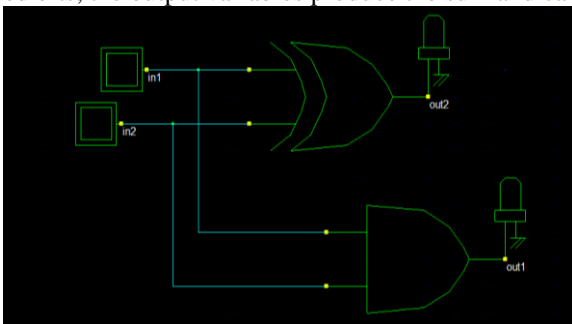


Fig. 1: half adder design

Inputs		Outputs	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 1: Truth table of half adder

The simplified Boolean function according to the truth

III. HALF ADDER USING MUX DESIGN

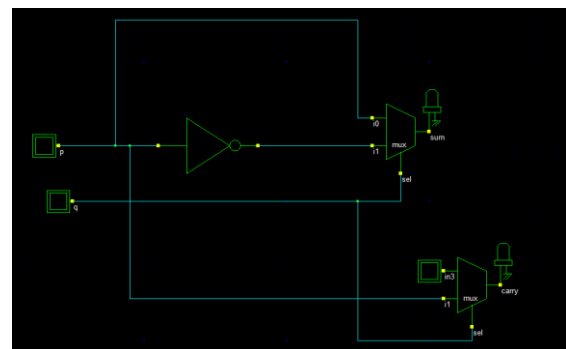


Fig. 4: half adder using mux design

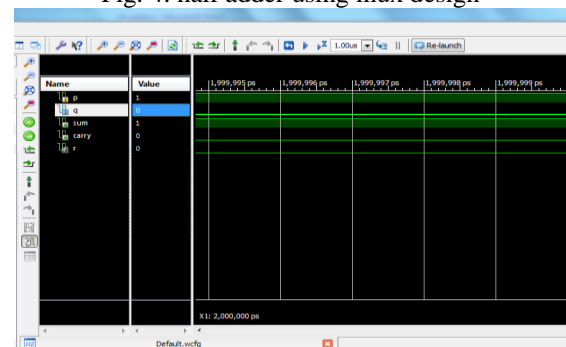


Fig. 5: simulation result of half adder using MUX on ISE Design Suite

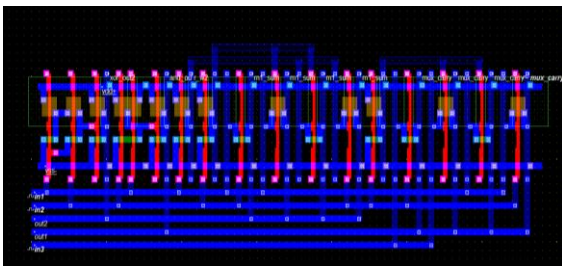


Fig. 6: Full automatic layout design of half adder using MUX

IV. HALF ADDER USING NAND GATES

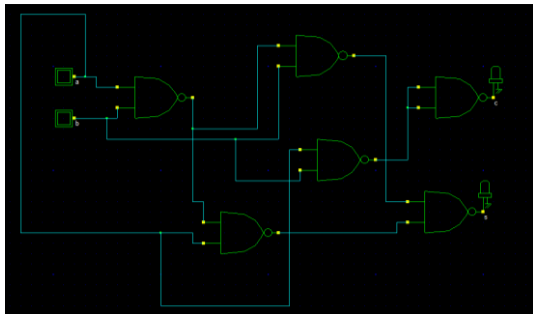


Fig. 7: half adder using NAND design

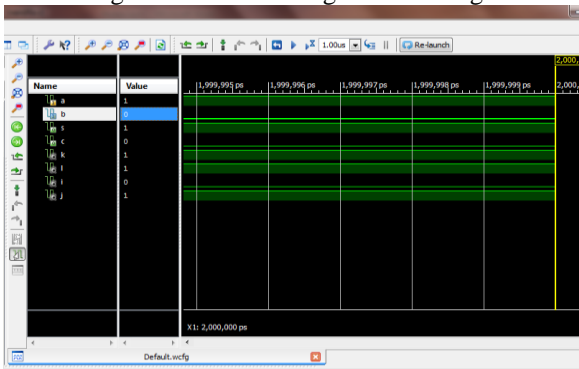


Fig. 8: simulation result of half adder using NAND on ISE Design Suite

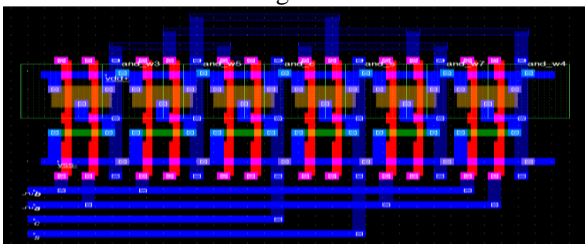


Fig. 9: Full automatic layout design of half adder using NAND gate

V. FULL ADDER DESIGN

A full adder can add a bit carried from another addition as well as the two inputs, whereas a half adder can only add the inputs together.

$$\text{Sum} = A \oplus B \oplus C$$

$$\text{Carry} = AB + BC + CA$$

A	B	Carry-In	Sum	Carry-Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 2: Truth table of full adder

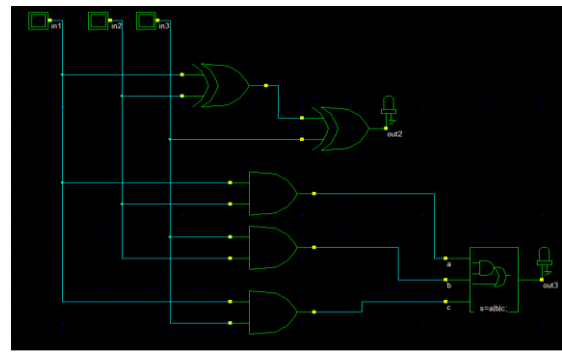


Fig. 10: fulladder design

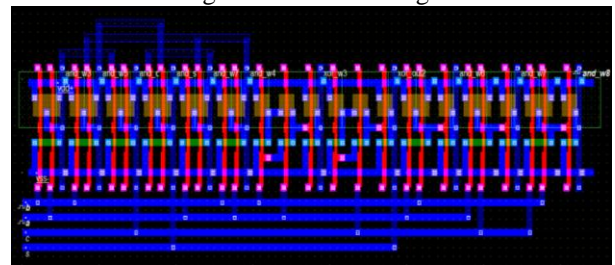


Fig. 11: Full automatic layout design of full adder

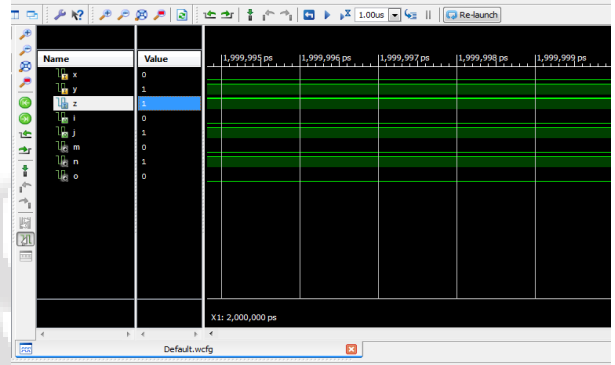


Fig. 12: simulation result of full adder

VI. FULL ADDER DESIGN USING MUX

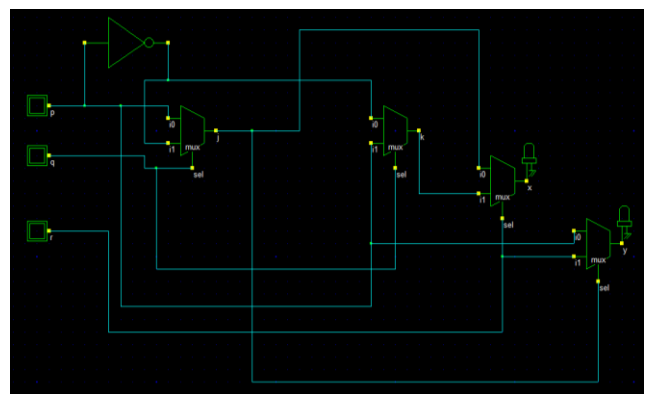


Fig. 13: full adder using MUX design

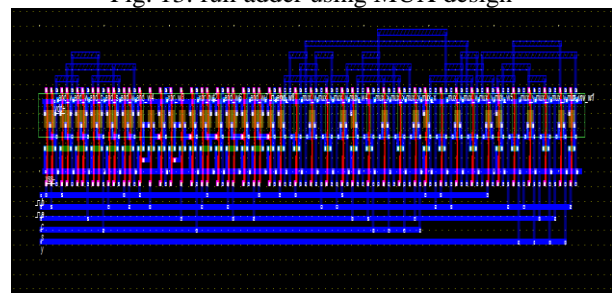


Fig. 14: Full automatic layout design of full adder using MUX

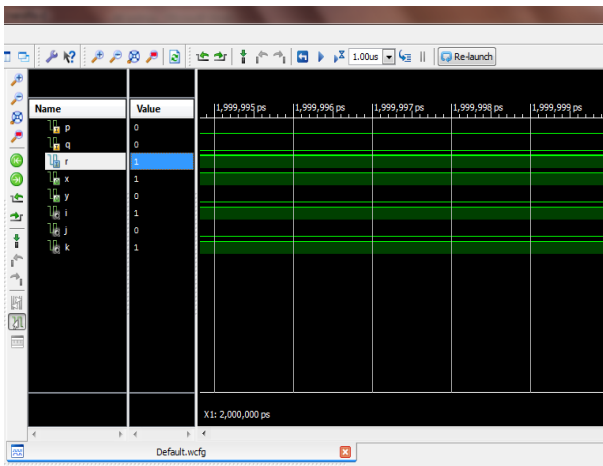


Fig. 15: simulation result of full adder using MUX on ISE Design Suite

VII. FULL ADDER DESIGN USING NAND GATE

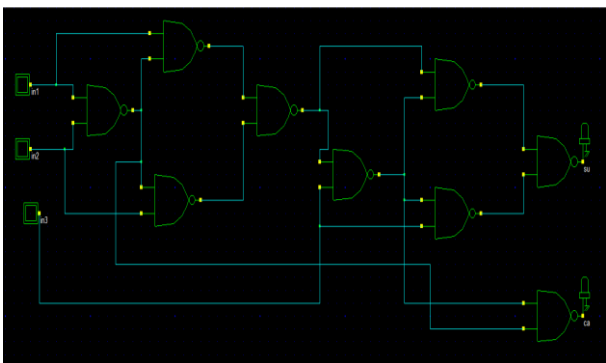


Fig. 16: full adder using NAND design

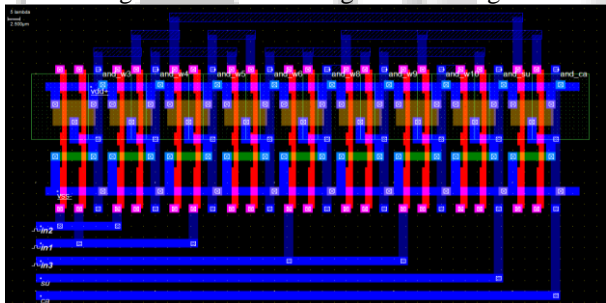


Fig. 17: Full automatic layout design of full adder using NAND gate

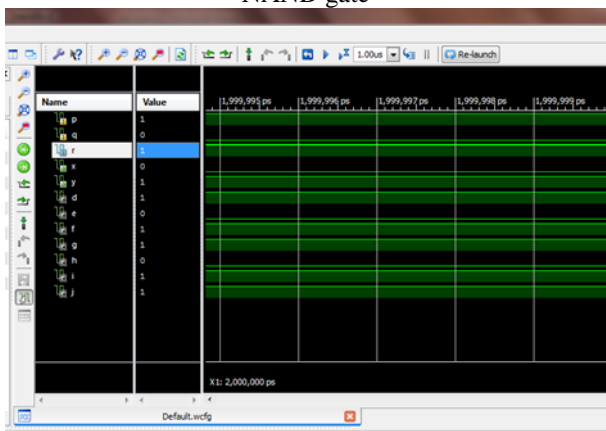


Fig. 18: simulation result of full adder using NAND on ISE Design Suite

VIII. RESULT ANALYSIS

Comparative analysis between two types of design method half adder and full adder using NAND gate and MUX is shown in table-2. Comparison aspects are based on CPU time, surface area used. Comparison shows that MUX based half adder and full adder is better than using gate.

Parameters	Ordinary HA		Using NAND		Using MUX	
	LUT'S	CPU time (s)	LUT'S	CPU time (s)	LUT'S	CPU time (s)
HA	2	4.07	2	2.82	1	2.48
FA	3	4.40	3	2.58	2	2.43

Table-2 Comparative Analysis

Thus chart-1, chart-2 and show the comparison graph for CPU time consumption of half adder and full adder using NAND,MUX

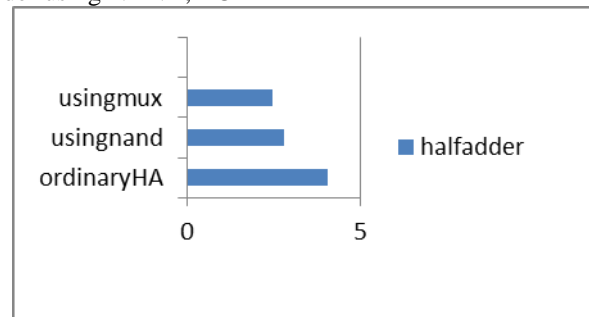


Fig. 18: Chart-1: CPU time of half adder comparison between design-1, design-2 and design-3

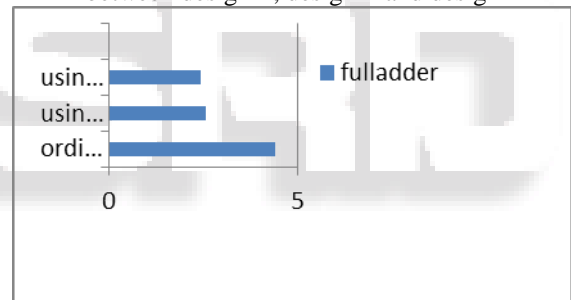


Fig. 20: Chart-2: CPU time of full adder comparison between design-1 design-2 and design-3

IX. CONCLUSION

From the above discussion we can conclude that adders using MUX is very useful technique to reduce the surface area on a chip and time consumption. So, there is a need for MUX design analysis and find better result for all parameters point of view. Numerically CPU time consumption and area is reduced by twice the amount. Time and area utilization of adders using NAND gate is 5% and MUX is producing 9%. The adder using NAND and MUX has been verified using Xilinx and the layout has been designed using MICROWIND EDA tool.

This adder's are also designed using different logic styles like static complementary logic, domino logic etc. These designs can used analog to digital converter for obtaining high speed, low power, minimum area.

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