Design of 4 Bit Johnson Counter using Reduced Number of Reversible Logic Gates

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Abstract— Over the last few decade reversible logic circuits have attracted considerable attention in improving some fields like nanotechnology, quantum computing, cryptography, optical computing and low power design of circuits due to its low power dissipating characteristic. In this paper we proposed the design of 4-bit Johnson counter with reduced number of reversible gates and derived with constant inputs, garbage output and number of gates to implement it.

Key words: Reversible Logic, Quantum Cost, Constant Input, Garbage Output, Delay, Johnson Counter

I. INTRODUCTION

Landauer states that the loss of one bit of information dissipates KTln2 joules of energy, where K is the Boltzmann constant and T is the absolute temperature at which the operation is performed [1]. At room temperature the heat dissipation due to loss of one bit of information is very small but not negligible. This computation procedure is irreversible. Further Bennett, showed that one can avoid KTln2 joules of energy dissipation from the circuit if input can be extracted from output and it would be possible if and only if reversible gates are used [2]. Research is going on in the field of reversible logic and a good amount of research work has been carried out in the area of reversible combinational logic. However, there is not much work in the area of sequential circuit like flip-flops and counters. A counter, by function, is a sequential circuit consisting a set of flip-flops connected in a suitable manner to count the sequence of the input pulses presented to it in digital form [6]. This paper proposes a advanced design of 4-bit Johnson or Shift counter using minimum number of reversible gates.

II. BASIC CONCEPTS

This section explains some basic concepts of reversible gates and quantum circuits which are as follows:

A. Reversible Logic Function

It is an n-input n-output logic function in which there is a one-to-one correspondence between the inputs and the outputs, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs.[4] This prevents the loss of information which is the root cause of power dissipation in irreversible logic circuits. Energy dissipation can be reduced or even eliminated if computation becomes Information-lossless. The reversible logic circuits must be constructed under two main constraints. They are:

- Fan-out is not permitted.
- Loops or feedbacks are not permitted

Quantum logic gates have some properties as shown in "(1)."

$$\left.\begin{array}{c} V \times V = NOT \\ V \times V^{+} = V^{+} \times V = I \\ V^{+} \times V^{+} = NOT \end{array}\right\} \ldots\ldots\ldots\ldots 1$$

Any reversible logic gate (circuit) is realized by using mentioned gates above, NOT and FG gates. The properties above show that when two V gates are in series they will behave as a NOT gate. Similarly, two V^+ gates in series also function as a NOT gate. A V gate in series with V^+ gate, and vice versa, is an identity.

B. Garbage Output

This refers to the number of unused outputs present in a reversible logic. A garbage output is an output that is needed to change an irreversible gate to a reversible one and are not used to the input to the other gates

C. Quantum Gate

Quantum gates are reversible and based on quantum computing [5]. For realizing 1×1 and 2×2 quantum gates we can use quantum technique. Since bigger quantum gates like 3×3, 4x4 etc. cannot be realized by quantum technique directly, 1×1 and 2×2 quantum gates are used for realizing this bigger quantum gates.

D. Quantum Cost

This refers to the cost of the circuit in terms of the cost of a primitive gate. The quantum cost of a reversible gate is the number of 1x1 and 2x2 reversible gates or quantum gates required in its design. The quantum costs of all reversible 1x1 and 2x2 gates are taken as unity. Since every reversible gate is a combination of 1 x 1 or 2 x 2 quantum gate, so the quantum cost of a reversible gate can be calculated by counting the numbers of NOT, Controlled-V, Controlled-V^+ and CNOT gates used[3].

E. Delay

The delay of a logic circuit is the maximum number of gates in a path from any input line to any output line. The definition is based on two assumptions: (i) Each gate performs computation in one unit time and (ii) all inputs to the circuit are available before the computation begins.

F. Reversible Gate

A gate with equal number of input and output in which input and output have one –to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. If the input vector of a reversible gate is denoted by $I_V= (I_1,I_2,I_3,\ldots,I_K)$, the output vector can be represented as $O_V= (O_1,O_2,O_3,\ldots,O_K)$. A reversible gate can be represented as K×K in which the number of input and output is K[7].

G. DF Gate (DFG)

Fig. 1 shows the block diagram of DF gate[9]. Fig.2(a) and fig. 2(b) shows the functionality of the DF gate. When control input A is equal to zero, clock input is directly

passed to the output P. Outputs Q and R are same and equal to Qn+1, where Q acts as present stage output and R is fed back to the input. When A is equal to one, Here clock input is directly passed to the output P. Output Q is equal to Qn+1' and R is Qn+1.

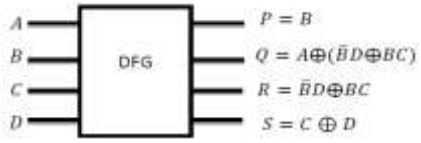

Fig. 1: Block diagram of DF gate

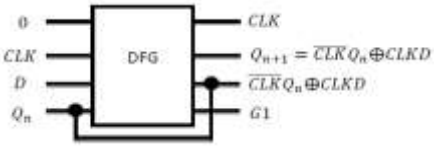

Fig. 2 (a) DF gate as D flip-flop with A=0

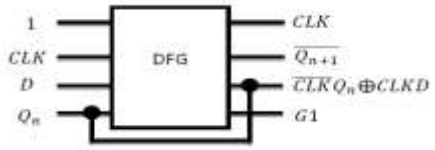

Fig. 2(b) DF gate as D flip-flop with A=1

III. PROPOSED WORK

A. *Johnson Counter*

The shift or Johnson counter is constructed by connecting the inverted output of the last flip-flop to the input of the first flip-flop. The truth table given in Table-I, one can observe that, for a 4-bit Johnson counter, there are 8-states. In general, an n-flip-flop shift counter will result in 2n states or Modulo-2n counter[8].

CLK	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0
1	1	0	0	0
1	1	1	0	0
1	1	1	1	0
1	1	1	1	1
1	0	1	1	1
1	0	0	1	1
1	0	0	0	1
1	0	0	0	0

Table 1: Truth table of 4-bit Johnson counter

B. *Proposed Design of Johnson Counter*

"Fig. 3" shows the proposed design of Johnson counter using DF gate.

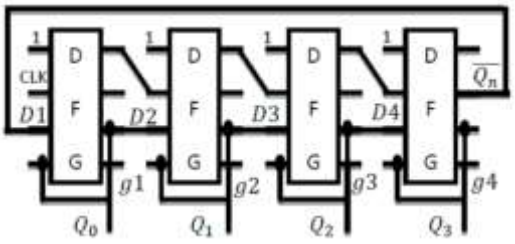

Fig. 3: Proposed Design of Johnson Counter.

IV. RESULTS AND DISCUSSION

In the implementation of 4-bit Johnson counter we use four SAM gate having Quantum cost (QC) of 4 and four DFG gate having Quantum cost =2. Number of gates, constant inputs, garbage output and quantum cost are shown in Table-II.

	No of Gates	No. of constant input	No. of garbage output	Delay
Proposed	4	5	4	4
Existing	8	8	4	8

Table 2: Results

V. CONCLUSION

We have presented the basic concepts of multipurpose binary reversible gates. Such gates can be used in regular circuits realizing Boolean functions. This paper proposes designs of basic reversible sequential elements such as flip-flops and four bit reversible Johnson or Shift Counter. In this paper, we implement a Johnson counter design directly from reversible gates. Minimization of Quantum cost, garbage output and number of gate is a challenging one. Here in this paper the proposed designs are better in terms of quantum cost and garbage outputs. The proposed design can have great impact in quantum computing. The proposed synchronous counter designs have the applications in building reversible ALU, nanotechnology, low power circuit design, cryptography, optical computing etc.

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