Improved Design of MOD-8 Synchronous UP/DOWN Counter using Reversible Gate

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Abstract— The Reversible logic synthesis techniques will definitely be a necessary part of the long-term future of computing due to its low power dissipating characteristic. Reversible logic gates are very much in demand for the future computing technologies as they are known to produce zero power dissipation under ideal conditions. Today, reversible logic circuits have attracted considerable attention in improving some fields like nanotechnology, quantum computing, and low power design of circuits. In this paper we proposed the design of MOD-8 synchronous up/down counter having reduced quantum cost, constant inputs and less number of gates to implement it using existing reversible gates.

Key words: Reversible Logic, Quantum Cost, Constant Input, Garbage Output, Synchronous Counter

I. INTRODUCTION

Landauer states that the loss of one bit of information dissipates KTln2 joules of energy, where K is the Boltzmann constant and T is the absolute temperature at which the operation is performed [1]. At room temperature the heat dissipation due to loss of one bit of information is very small but not negligible. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components. This computation procedure is irreversible. Further Bennett, showed that one can avoid KTln2 joules of energy dissipation from the circuit if input can be extracted from output and it would be possible if and only if reversible gates are used [2]. Research is going on in the field of reversible logic and a good amount of research work has been carried out in the area of reversible combinational logic. However, there is not much work in the area of sequential circuit like flip-flops and counters. A counter is a sequential circuit capable of counting the number of clock pulses that have arrived at its clock input. This paper proposes the design of MOD-8 synchronous up/down counter having reduced quantum cost, constant inputs and less number of gates to implement it using existing reversible gates.

II. BASIC CONCEPTS

This section explains some basic concepts of reversible gates and quantum circuits which are as follows:

A. Reversible Logic Function

It is an n-input n-output logic function in which there is a one-to-one correspondence between the inputs and the outputs, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs.[6] This prevents the loss of information which is the root cause of power dissipation in irreversible logic circuits. Energy dissipation can be reduced or even eliminated if computation becomes Information-lossless. The reversible logic circuits must be constructed under two main constraints. They are:

- Fan-out is not permitted.
- Loops or feedbacks are not permitted

Quantum logic gates have some properties as shown in "(1.1)."

$$\left.\begin{array}{c} V \times V = NOT \\ V \times V^{+} = V^{+} \times V = I \\ V^{+} \times V^{+} = NOT \end{array}\right\} \ldots\ldots(1.1)$$

Any reversible logic gate (circuit) is realized by using mentioned gates above, NOT and FG gates. The properties above show that when two V gates are in series they will behave as a NOT gate. Similarly, two V^+ gates in series also function as a NOT gate. A V gate in series with V^+ gate, and vice versa, is an identity.

B. Garbage Output

This refers to the number of unused outputs present in a reversible logic. A garbage output is an output that is needed to change an irreversible gate to a reversible one and are not used to the input to the other gates

C. Quantum Gate

Quantum gates are reversible and based on quantum computing. For realizing 1×1 and 2×2 quantum gates we can use quantum technique. Since bigger quantum gates like 3×3, 4x4 etc. cannot be realized by quantum technique directly, 1×1 and 2×2 quantum gates are used for realizing this bigger quantum gates.

D. Quantum Cost

This refers to the cost of the circuit in terms of the cost of a primitive gate. The quantum cost of a reversible gate is the number of 1x1 and 2x2 reversible gates or quantum gates required in its design. The quantum costs of all reversible 1x1 and 2x2 gates are taken as unity. Since every reversible gate is a combination of 1 x 1 or 2 x 2 quantum gate, so the quantum cost of a reversible gate can be calculated by counting the numbers of NOT, Controlled-V, Controlled-V^+ and CNOT gates used.[3],[14]

E. Reversible Gate

A gate with equal number of input and output in which input and output have one –to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. If the input vector of a reversible gate is denoted by I_V= (I_1,I_2,I_3,…,I_K), the output vector can be represented as O_V= (O_1,O_2,O_3,…,O_K). A reversible gate can be represented as K×K in which the number of input and output is K.

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F. Delay

The delay of a logic circuit is the maximum number of gates in a path from any input line to any output line. The definition is based on two assumptions: (i) Each gate performs computation in one unit time and (ii) all inputs to the circuit are available before the computation begins.

G. Feynman Gate (CNOT Gate)

The Feynman gate (FG) or the Controlled-NOT gate (CNOT) is a 2-input 2- output reversible gate having the mapping (A, B) to (P = A, Q = A⊕B) where A, B are the inputs and P, Q are the outputs, respectively.[5]. Since it is a 2×2 gate, it has a quantum cost of 1. "Fig. 1" and "Fig. 2" shows the block diagram and quantum representation of the Feynman gate.

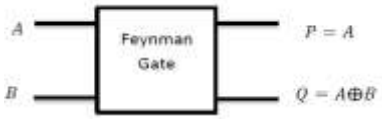

Fig. 1: 2X2 Feynman

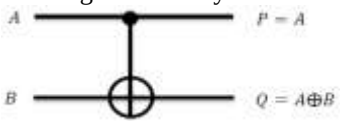

Fig. 2 Quantum representation of Feynman

H. SAM Gate

Input vector I_v and Output vector O_v are represented as I_v=(A,B,C) and O_v= $P = \bar{A}, Q = \bar{A}B \oplus A\bar{C}, R = \bar{A}C \oplus AB$ and respectively. The block diagram of 3x3 SAM gate is shown in "Fig. 3" and its quantum representation is shown in "Fig. 4". The quantum cost of SAM gate is 4. [4],[9]

Fig. 3: Block diagram of 3x3 SAM Gate

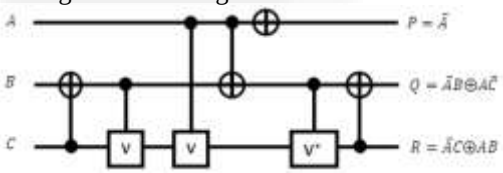

Fig. 4: Quantum representation of SAM gate.

If we give 0 to 3rd input then we get NOT of 1st input in 1st output, OR of 1st and 2nd inputs in 2nd output and AND of 1st and 2nd inputs in 3rd output. This operation is shown in "Fig. 5". So this gate can be used as two input universal gate.

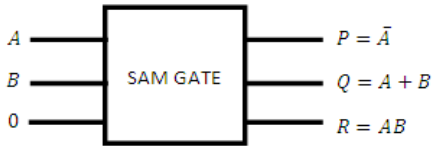

Fig. 5: SAM as NOT, OR and AND.

I. Clocked T-Flip –Flop

The characteristic equation of a clocked T flip-flop [10] is $Q = (T \oplus Q).CLK \oplus \overline{CLK}.Q$. The equation can be simplified as $Q = (T.CLK) \oplus Q$. This clocked flip-flop is realized by a Peres gate and a Feynman gate as shown in "Fig. 6". [9]-[13]

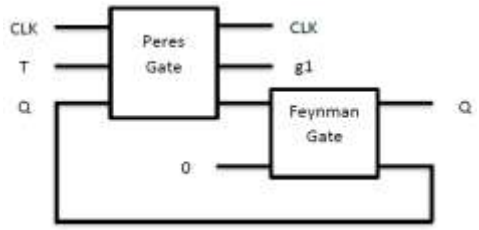

Fig. 6: T Flip-Flop using Peres and Feynman gate

III. PROPOSED WORK

A. Mod 8 Up/Down Synchronous Counter

The Block diagram of 3-bit Up/Down counter is shown in "Fig. 7"

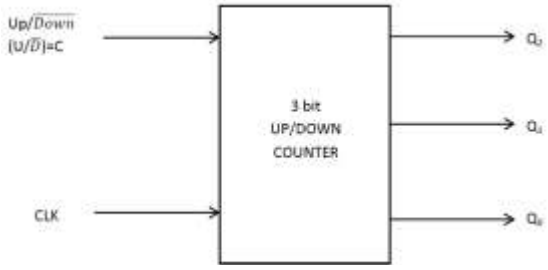

Fig. 7: Block diagram of 3-bit Up/Down counter

From "Fig. 7", when Up/$\overline{Down}$ =1, the counter will work in the Up mode, i.e. it counts from state 000 to state 111. when Up/$\overline{Down}$ = 0, it will work in the down mode, i.e. it counts from state 111 to state 000.

The excitation table having entries for flip-flop inputs (T_2, T_1 and T_0) can be drawn, as shown in Table -1, with the help of present state – next state table and excitation table of T flip-flop.

Control Input	Present State			Next State			Excitation Inputs		
C=U/D'	q_2	q_1	q_0	Q_2	Q_1	Q_0	T_2	T_1	T_0
0	0	0	0	1	1	1	1	1	1
0	0	0	1	0	0	0	0	0	1
0	0	1	0	0	0	1	0	1	1
0	0	1	1	0	1	0	0	0	1
0	1	0	0	0	1	1	1	1	1
0	1	0	1	1	0	0	0	0	1
0	1	1	0	1	0	1	0	1	1
0	1	1	1	1	1	0	0	0	1
1	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	1
1	0	1	0	0	1	1	0	0	1
1	0	1	1	1	0	0	1	1	1
1	1	0	0	1	0	1	0	0	1
1	1	0	1	1	1	0	0	1	1
1	1	1	0	1	1	1	0	0	1
1	1	1	1	0	0	0	1	1	1

Table 1: Excitation table for MOD-8 UP/DOWN Counter

Derived Equations for T_2, T_1, T_0, are as follows:

$T_2 = \bar{C}\,\overline{q_1}\,\overline{q_0} + C\,q_1\,q_0$ ..... Equation 2

$T_1 = \bar{C}\overline{q_0} + Cq_0$ ..... Equation 3

T_0=1 ..... Equation 4

Implementation of these derived equations 2, 3 and 4 are shown in our proposed design in Figure 13 of MOD-8 UP/DOWN Synchronous Counter using reversible gates Feynman, Peres, SAM and Toffoli gate (4X4).

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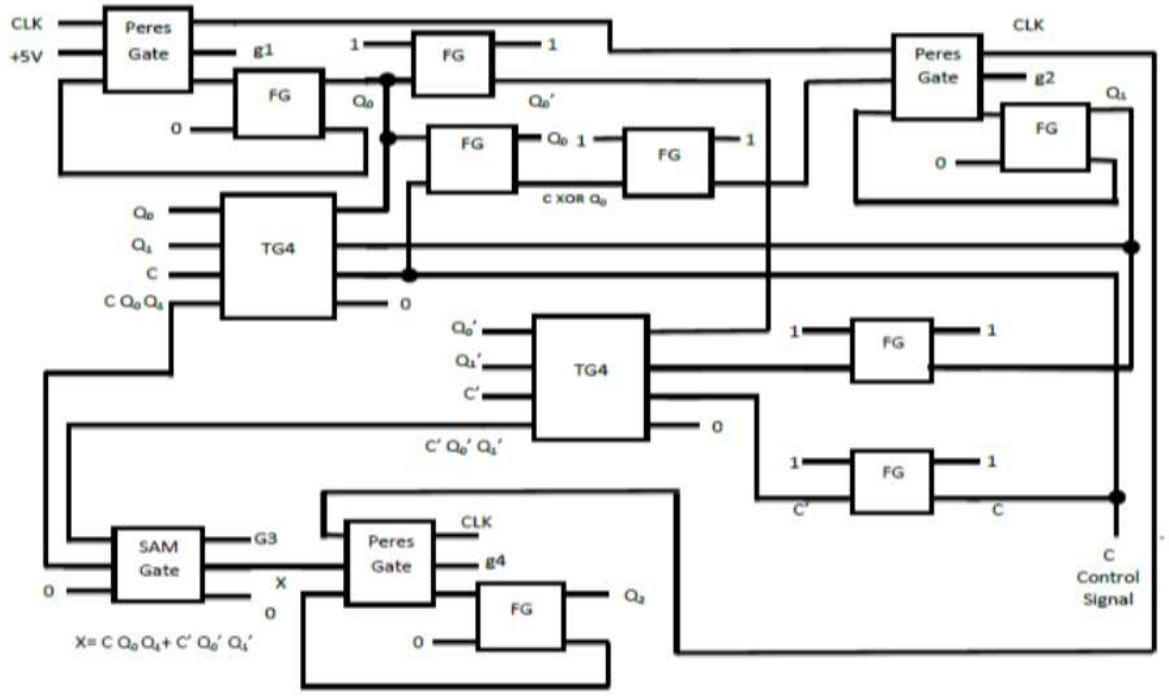

Fig. 9: Proposed Design of MOD-8 Synchronous Up/Down Counter

IV. Results and Discussion

In the implementation of MOD-8 UP/DOWN Synchronous counter we use three Peres gate having QC=4, eight Feynman gate having QC=1, two Toffoli gate (4X4) having QC=13 . one SAM gate having QC=4. Number of gates , constant inputs, garbage output and quantum cost are shown in Table 2.

Parameters	Existing [15]	Proposed Design
No of Gates	17	14
No. of constant input	13	12
No. of garbage output	5	4
Quantum cost	53	50

Table 2: Results

V. Conclusion

We have presented the basic concepts of multipurpose binary reversible gates. Such gates can be used in regular circuits realizing Boolean functions. This paper proposes improved design three bit reversible synchronous up/down counter which requires less no. of gates, Quantum Cost Minimization of Quantum cost, garbage output and number of gate is a challenging one. Here in this paper the proposed designs are better in terms of quantum cost and garbage outputs. The proposed design can have great impact in quantum computing. The proposed synchronous counter designs have the applications in building reversible ALU, reversible processor, nanotechnology, low power circuit design etc.

Acknowledgement

The authors wish to thank ECE department of NSHM Knowledge Campus Durgapur-GOI, West Bengal, India for supporting this work.

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