Dual Active Clamped DC-DC Converter for Low Voltage Photovoltaic Sources

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Abstract— The photovoltaic (PV) module-integrated converter (MIC) system is the key technology for the future distributed production of electricity using solar energy. The PV MIC system offers "plug and play" concept, greatly optimizing the energy yield from the PV module[1-3]. Each PV module has its own power conversion system, generating the maximum power from the PV module. To make the PV MIC system commercially viable, a low-cost and high-efficiency power conversion scheme should be developed. This project proposes a Dual active clamped dc–dc converter with fast dynamic response for low-voltage PV sources. An improved active-clamped dc–dc converter is presented by using a dual active-clamping circuit. The voltage tension at power switches can be reduced at low-voltage side. Also, a modified proportional integral (PI) controller is suggested for fast output voltage control. The performance of the proposed converter is verified using simulation using PSIM software for the output power of 200 watts.

Key words: Zero Voltage Switching, Zero Current Switching, PI controller, Photo Voltaic Cell, DC-DC converter

I. INTRODUCTION

The sun is almost an inexhaustible source of energy capable of supplying large amounts of energy. The total amount of solar energy absorbed by the desert area in six hours is comparable to the total global energy consumption in an entire year. This large amount of solar energy incident on the earth remains unharnessed. Photovoltaic (PV) technology converts solar energy into electrical energy. The basic element of PV technology is the solar cell. A solar cell consists of a p-n junction fabricated in a thin wafer of layer of semiconductor similar to a diode. When exposed to light, photons energy is greater than depletion layer energy of the semiconductor. It will create an electron-hole-pair generation So the current will flows in the circuit is proportional to the incident radiation. Workable voltage and reasonable power is obtained by inter connecting appropriate number of cells. This assembly is known as solar module, a basic building block of a PV system.

The PV module voltage has a low-voltage characteristic [5].In order to deliver electric power into the grid, the low PV module voltage should be converted into a high dc voltage [6]. Thus, a dc–dc converter with a high-voltage gain is needed. The active-bridge dc–dc converter has been used for low-voltage PV sources [7], [8]. The power switches at low-voltage side are turned ON at zero voltage. However, the output diode at high-voltage side has high switching power losses due to its reverse-recovery current [9]. The half-bridge dc–dc converter has been presented to reduce switching power losses at high voltage side [10]. The output diodes are turned OFF at zero current by using the voltage doubler rectifier. However, an additional un controlled rectifier is needed, which increases switching power losses. Alternatively, the active-clamped dc–dc converter has been used for low-voltage PV sources [11], [12]. It uses the active-clamping circuit and the resonant voltage doubler rectifier. However, the active-clamping circuit increases the voltage stress of power switches at low-voltage side, causing high switching power losses.

Considering the dynamic response of the converter, bandwidth limitations of conventional controllers have forced power electronics engineers to increase switching frequency or increase output capacitor [13]. This paper proposes a Dual active clamped dc–dc converter for low-voltage PV sources. The voltage stress of power switches can be reduced at low-voltage side. Also, a modified proportional and integral (PI) controller is suggested for fast output voltage control. The transient performance of the proposed converter is improved. The proposed converter is realized with minimal hardware with a low cost. The performance of the proposed converter is verified using a 200-W experimental prototype.

II. CONVERTER OPERATION

Fig. 1 shows the circuit diagram of the proposed dc–dc converter. The converter consists of main switches (S_1, S_4), the dual active-clamping circuit (S_2, S_3, C_c), the transformer T, and the resonant voltage doubler rectifier (L_{lk}, C_r, $D_{o\,1}$, $D_{o\,2}$). The main switches (S_1, S_4) and auxiliary switches (S_2, S_3) operate complementarily with a short dead time. All switches are the metal–oxide–semiconductor field-effect transistors. C_i is the input capacitor. C_c is the clamping capacitor. C_o is the output capacitor. The capacitors C_i, C_c, and C_o are large enough so that their voltages V_i, V_c, and V_o are considered constant, respectively. The transformer T has the magnetizing inductor Lm and leakage inductor L_{lk} with the turns ratio of 1:N, where $N=N_s/N_p$. L_{lk} is assumed to be much smaller than Lm.

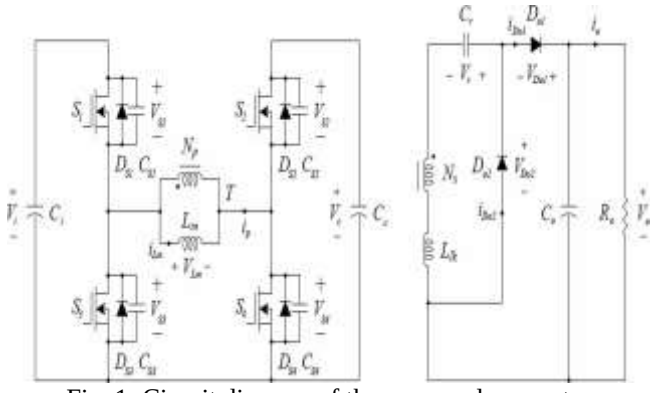

Fig. 1: Circuit diagram of the proposed converter

The capacitor C_r is the resonant capacitor. C_r resonates with the leakage inductor L_{lk}. Thus, the resonant capacitor voltage V_r is not considered constant for one switching period.

Fig. 5 shows the switching waveforms of the proposed converter during one switching period Ts (=1/f_s). Fig. 5(a) shows the switching waveforms at the primary side current and current in the magnetizing current. Fig. 5(b) shows the switching waveforms at the secondary side. The proposed converter has six switching modes during T_s. The duty ratio D is based on the on-time of the main switches. Fig. 3 shows the switching modes of the proposed converter during T_s. Before t = t0, S_2 and S_3 have been turned OFF. The voltages $V_{S\,1}$ and $V_{S\,4}$ have been zero when the primary current i_p flows through the body diodes $D_{S\,1}$ and $D_{S\,4}$.

Mode 1 [t0, t1]: At t = t0, S1 and S4 are turned ON. Since VLm = vi, the magnetizing inductor current iLm increases linearly as [14].

$$i_{lm}(t) = i_{lm}(t_o) + \frac{V_i}{L_m}(t - t_o) \qquad (1)$$

At the secondary side, Nvi is applied to the secondary winding of T. The output diode Do1 is turned ON. The series-resonant circuit consisting of L_{lk} and C_r is formed by the series resonance between L_{lk} and C_r, the energy stored in Cr is transferred to Co. The angular resonant frequency ωr of the series-resonant circuit is

$$\omega_r = 2\pi f_r = \frac{1}{\sqrt{L_{lk}C_r}} \omega_r = 2\pi f_r = \frac{1}{\sqrt{L_{lk}C_r}} \qquad (2)$$

Where fr is the resonant frequency. The primary current ip is expressed as

$$i_p(t) = i_p(t_o) + \frac{V_i}{L_m}(t - t_0) + N i_{Do1}(t) \qquad (3)$$

where the output diode current iDo1 is given by

$$i_{Do1} = \frac{V_o - NV_i - V_r}{Z_r} \sin\omega_r(t - t_o) \qquad (4)$$

Mode 2 [t1, t2]: At t = t1, the half-resonant period of the series resonance is finished. The output diode current iD_{o1} is zero before D_{o1} is turned OFF. D_{o1} can be turned off at zero current without any diode reverse recovery current.

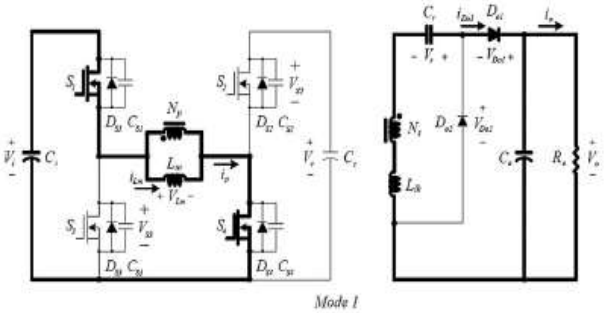

Fig. 2: Mode1 operation of converter

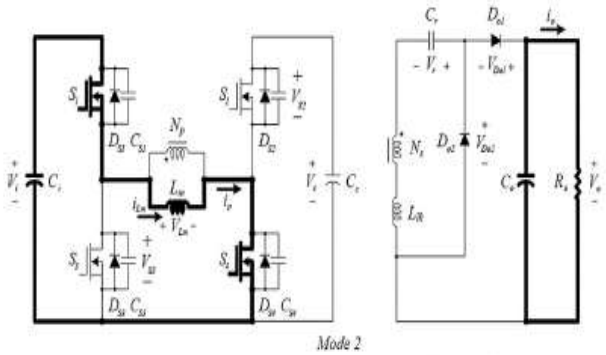

Fig. 3: Mode 2 operation of converter

Mode 3 [t_2, t_3]: At t = t_2 , S_1 and S_4 are turned OFF. The primary current i_p charges $C_{S\,1}$ and $C_{S\,4}$ and discharges $C_{S\,2}$ and $C_{S\,3}$. V_{S1} and V_{S4} increase from zero to V_i . $V_{S\,2}$ and $V_{S\,3}$ decrease from V_c to zero. Since the switch capacitor C_S (= $C_{S\,1}$ = $C_{S\,2}$ = $C_{S\,3}$ = $C_{S\,4}$) is very small, so this mode is appear only small period.

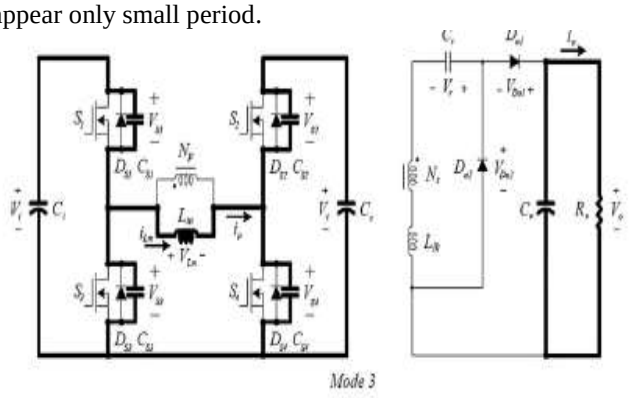

Fig. 4: Mode 3 operation of converter

Mode 4 [t3, t4]: At t = t3, S2 and S3 are turned ON. Since V_{Lm} = –V_c, the magnetizing inductor current i_{Lm} decreases linearly as given by

$$i_{Lm}(t) = i_{Lm}(t_3) - \frac{V_c}{L_m}(t - t_3) \qquad (6)$$

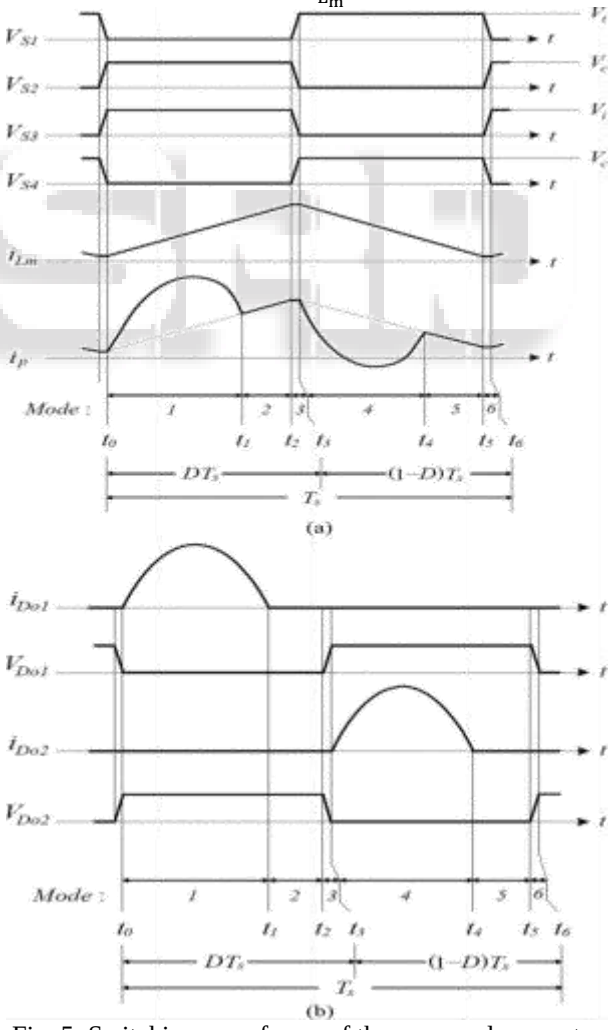

Fig. 5: Switching waveforms of the proposed converter during Ts : (a) waveforms at the primary side and (b) waveforms at the secondary side.

At the secondary side, N*V_c is reversely applied across the secondary winding of T. The output diode $D_{o\,2}$ is

turned ON. The series-resonant circuit consisting of L_{lk} and C_r is formed again.

The input power is transferred to C_r by the series resonance between L_{lk} and C_r. By referring the output diode current i_{Do2} to the primary side, the primary current ip is expressed as

$$i_p(t) = i_p(t3) - \frac{V_c}{L_m}(t - t_3) - Ni_{Do2}(t) \quad (7)$$

The diode ID02 current is written as

$$i_{Do2}(t) = \frac{NV_c + V_r}{Z_r} \sin\omega_r(t - t_3) \quad (8)$$

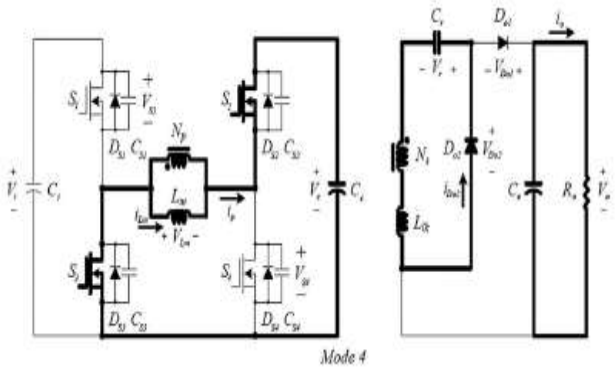

Fig. 6: Mode 4 operation of converter

Mode 5 [t_4, t_5]: At t = t_4, the half-resonant period of the series resonance is finished. The output diode current i_{Do2} is zero before D_{o2} is turned OFF. D_{o2} can be turned OFF without any diode reverse-recovery current.

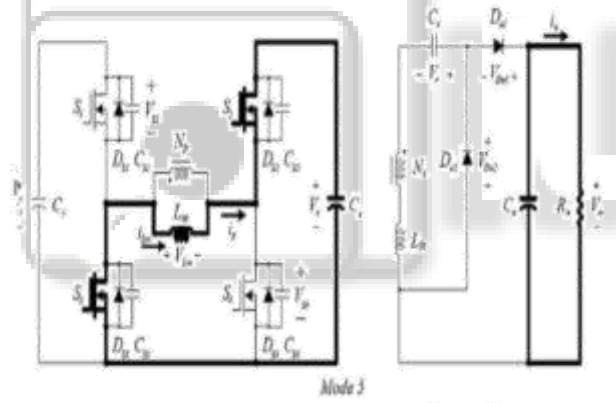

Fig. 7: Mode 5 operation of converter

Mode 6 [t5, t6]: At t = t5, S_2 and S_3 are turned OFF. The primary current i_p charges C_{S2} and C_{S3} and discharges $C_{S\,1}$ and C_{S4}. $V_{S\,2}$ and $V_{S\,3}$ increase from zero to V_c. V_{S1} and $V_{S\,4}$ decrease from V_i to zero. Since the capacitor CS is very small, so this mode is appear only small period .The next switching cycle begins when S_1 and S_4 are turned ON again.

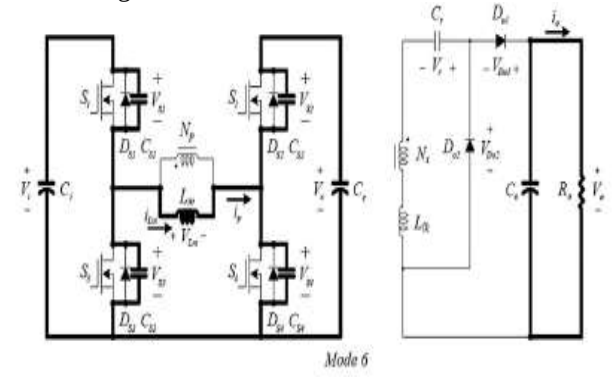

Fig. 8: Mode 6 operation of converter

III. CALCULATION OF CLAMPING CAPACITOR AND RESONANT CAPACITOR VOLTAGE

By the voltage-second balance relation on the magnetizing inductor Lm, the voltages V_c and V_r are expressed as

$$V_c = \frac{D}{1-D} V_i \quad (9)$$

$$V_r = (1 - D)V_o \quad (10)$$

For the voltage-second balance relation on the secondary winding of T during T_s, the following relation between the output voltage v_o and the input voltage v_i is obtained as

$$\frac{V_o}{V_i} = \frac{N}{1-D} \quad (11)$$

The maximum voltage stress of S_1 and S_3 is confined to the input voltage V_i. The voltage stress of S_2 and S_4 is confined to the clamping capacitor voltage V_c. The dual active-clamping circuit is used in the proposed converter. The clamping capacitor voltage is always lower than the clamping capacitor voltage in case of the active-clamping circuit. So that the switch voltage stress of the proposed converter is always lower than the switch voltage stress of the active-clamping circuit. Especially, when the duty ratio is below 50%, the clamping capacitor voltage is lower than the input voltage v_i applied to the converter circuit. It is critically beneficial in low-voltage PV applications where more than 50% of the power losses are lost as switching power losses. The output diode currents i_{Do1} and i_{Do2} should be zero before the output diodes D_{o1} and D_{o2} are turned off. The half-resonant period of the series resonance during Mode 1 and Mode 4 should be finished before the output diode is turned off.

IV. CONDITIONS FOR ZERO CURRENT TURN OFF OF THE DIODE

To obtain the zero-current turn-off of the output diode the following condition should be satisfied

$$\sin[\omega_c D_{max} Ts] = 0, \text{ if} D_{max} \leq 0.5 \quad (12)$$

$$\sin[\omega_c (1 - D_{max}) T_s] = 0, \text{ if} D_{max} > 0.5 \quad (13)$$

Where D_{max} is the maximum duty ratio ω_c is the critical angular resonant frequency as $\omega_c = 2\pi f_c$. f_c is the critical resonant frequency of the series-resonant circuit.

For zero-current turnoff of the output diode, the resonant frequency f_r should be higher than the critical resonant frequency f_c. Then, the resonant capacitor C_r should be determined as

$$c_r < \frac{1}{\omega_c^2 L_{lk}} \frac{D_{max}^2 T_s^2}{\pi^2 L_{lk}}, \quad (14)$$

$$= \frac{(1 - D_{max}^2)T_s^2}{\pi^2 L_{lk}} \quad (15)$$

V. CONTROLLER FOR THE PROPOSED CONVERTER

A. Calculation of Duty Ratio

From mode 4 and mode5 the magnetizing current i_{Lm} decreases linearly. The energy stored in L_m is transferred to C_c. The following voltage relation is obtained:

$$V_i - L_m \frac{diL_m}{dt} = 0 \quad (18)$$

$$V_i - L_m \frac{diL_m}{dt} - V_c = 0 \quad (19)$$

From (18) and (19), depending on the duty ratio D of the switches, the average magnetizing inductor voltage during Ts gives the following relation:

$$V_i DT_s + (V_i - V_c)(1 - D)T_s = L_m \Delta \qquad (20)$$

Then, the duty ratio D is represented by

$$D = D_n + D_c \qquad (21)$$

where D_n is a nominal duty ratio and Dc is a controlled duty ratio. The nominal duty ratio D_n and the controlled duty ratio D_c can be, respectively, represented as

$$D_n = 1 - \frac{NV_i}{V_o} \qquad (22)$$

$$D_c = \frac{NL_m \Delta i_{Lm}}{V_o T_s} \qquad (23)$$

Then, the duty ratio D becomes

$$D = D_n + D_c = 1 - \frac{NV_i}{V_o} + \frac{NL_m \Delta i_{Lm}}{V_o T_s} \qquad (24)$$

To regulate the output voltage for the output load variation, the conventional PI controller can be used for the controlled duty ratio Dc as

$$D_c = k_p e + k_i \int e \, dt \qquad (25)$$

$$e = V_o^* - V_o \qquad (26)$$

where V^*_o is the reference output voltage, e is the voltage error between V^*_o and V_o , and k_p and k_i are the PI control gains of the controller, respectively. The regulated output voltage is an important factor achieving high performance.

VI. SIMULATION OF THE DUAL ACTIVE CLAMPED DC-DC CONVERTER

The dual active clamped dc-dc converter consists of four switches, two diodes, one transformer and capacitors.

The simulation diagram of the proposed converter is shown in figure 9.

The duty ratio for the proposed converter is obtained by using the equation 24. And the proportional gain of the PI controller is obtained using the equation 23.

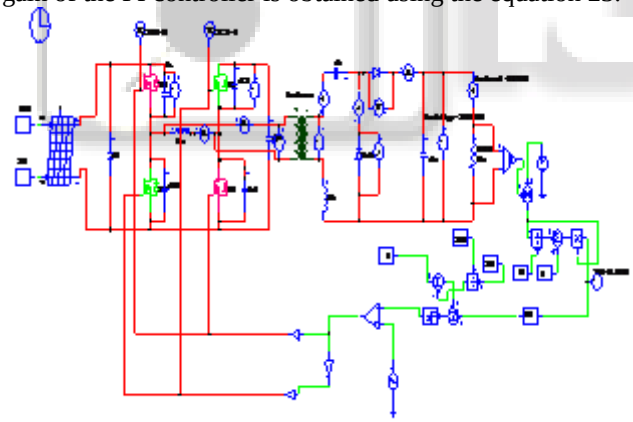

Fig. 9: Simulation diagram of proposed converter

$$k_P = \frac{NL_m}{V_o T_s} \qquad (27)$$

Next choosing of the integral gain plays the important role for maintains the stability of the converter. The large value of integral gain adversely affects the stability of the system. So the integral gain is set as small number. The final one is scaling factor. If the scaling factor is decreased the modified error is increased, which provides a fast dynamic response.

Fig. 12 shows the output diode voltages V_{Do1} and V_{Do2} and output diode currents i_{Do1} and i_{Do2} for the output load. The diode current flows in the circuit due to the series resonance between the leakage inductor and the resonant capacitor. The diode current increases as the output load increases. The diode current is zero before the output diode is turned OFF. Zero Current Switching of each output diode is achieved at its turn-off instance.

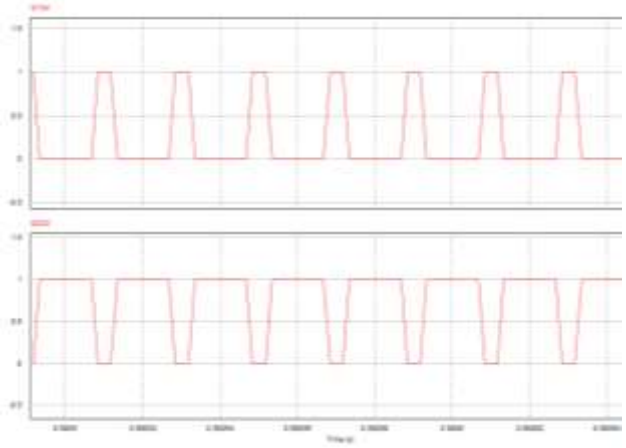

Fig. 10: Firing pulse applied to the converter gate circuit.

The magnetizing inductor current waveform is shown in fig.11.

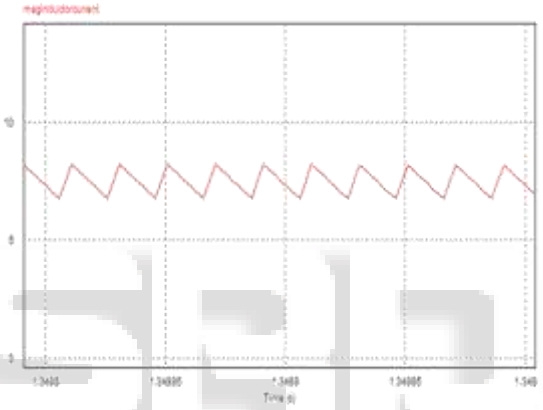

Fig. 11: Magnetizing current waveform

The switching power loss caused by the diode reverse recovery current can be removed by zero-current turn-off of the output diode.

The proposed converter achieves the highest efficiency for the rated output power. Switching power losses are reduced by decreasing the high voltage appeared across the power switches in the proposed converter. The power efficiency is increased by reducing switching power losses.

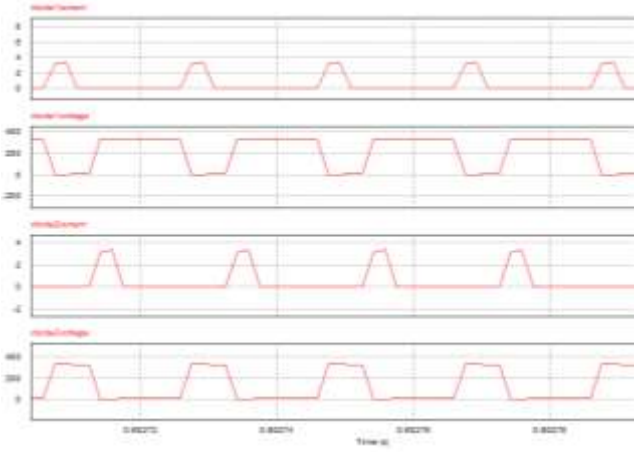

Fig. 12: Diode voltage and current waveform

The output voltge and current waveform of the proposed converter is shown in fig 13.

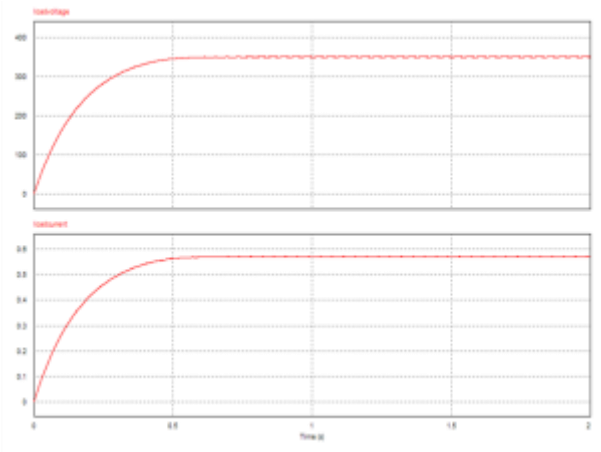

Fig. 13: Output voltage and current waveform

The below graph shows the efficiency comparision of the proposed converter using differet controller.

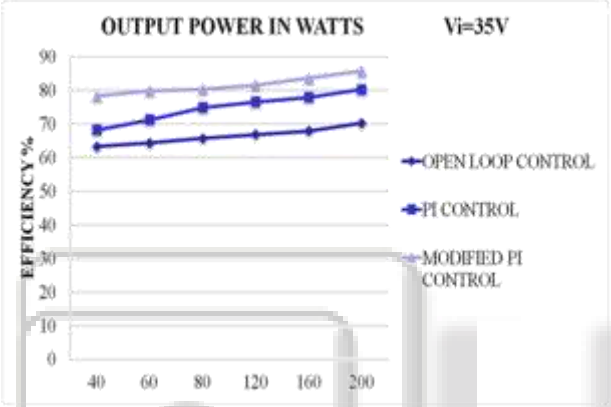

Fig. 14: Output Power

VII. CONCLUSION

The dual active clamped DC-DC converter has been implemented for low voltage PV sources. The proposed converter reduces the switching power losses, increases the power efficiency for the rated output power. The zero voltage switching reduces the switching losses in the low voltage side. In high voltage side the diode current becomes zero before the diodes are turned off and this reduces the stress across the diode. Modified PI controller has been used for fast output voltage control. Due to the advantages like reduced losses and high efficiency this converter has been used for the grid connected PV system. The proposed converter achieves the efficiency of 84.56% at the input voltage of 35 V for 200 watts output power.

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