FPGA based Single Phase Switched Capacitor Boost Multilevel Inverter

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Abstract— Using parallel-series converter in as DC Power supply appliance gives a good opportunity to maintain stable supply while the load is changing. In this report, a new boost switched capacitor multilevel inverter is proposed. It consists of two structures such as a switched capacitor circuit and a two level (full bridge) inverter which are connected in cascade. Here small input voltage can be used to produce a boosted output voltage. Number of switching devices used in the circuit is reduced as compared to the conventional cascaded multilevel inverter of same configuration. The multilevel dc output voltage of the switched capacitor circuit becomes the input voltage of the classical full bridge inverter, resulting in a staircase output voltage waveform. Such a multilevel waveform is close to a sinusoidal, its harmonic content can be reduced when compared to the conventional multilevel inverter by using the PWM control strategy. The control strategy is the key part for the proper working of this circuit and can be implemented by using field programmable gate arrays (FPGA) and by VHDL programming in Xilinix. This inverter outputs larger voltage than the input voltage by switching the capacitors in series and in parallel. The maximum output voltage is determined by the number of the capacitors. Unlike traditional multilevel inverters, this topology does not require an external voltage balancing circuit, a complicated control scheme or isolated dc sources to maintain its voltage levels while delivering sustained real power. In this report, the circuit configuration the theoretical operation, the simulation results with MATLAB/SIMULINK Ra2010a and experimental setup with Spartan 3 along with the results are shown.

Key words: FPGA – Field Programmable Gate Array, MLI-Multi Level Inverter, PWM –Pulse Width Modulation, SC-Switched Capacitor

I. INTRODUCTION

In recent years, electrical energy systems, electric vehicles, dispersed generation and renewable energy sources like PV, fuel cell etc. are focused plays a vital role against the global environmental issues. And with the rapid development in electro-technical fields, the power electronic devices (converters, inverters etc.) that are required for these systems are expected to handle the higher rating of voltage and capacity [1]-[4]. As a provision of this issue, multilevel inverters have gained much attention in recent years due to its advantage in high power with low harmonic applications.

Multilevel inverters have several advantages over the conventional inverters. One of the significant advantages of multilevel inverter configuration is the harmonic reduction in the output waveform without increasing the switching frequency or decreasing the inverter power output. The multilevel inverter has lesser harmonics compared to the conventional bipolar inverter output voltage. As the number of levels reach infinity, the output THD approaches zero. In normal condition when amplitude modulation index is one that time magnitude of output voltage of inverter is same as input

Voltage, So that we have to use dc/dc boost converter to increase output voltage levels to ensure output voltage is to be greater or at output side we have to use inductors or transformer but at higher power transformer should withstand heavy magnetic core so that it can sustain higher power which increases size of whole inverter assembly. There issues are considered since battery technologies haven't evolved too much. Almost in every application lead acid batteries have proven their potential at lower cost. By reducing size of inverter assembly we can increase the size of these batteries, which are in beneficial to end consumers of such products. As a provision against the issue, a charge pump, which does not have any inductors, is applied to such systems. A charge pump output a larger voltage than the input voltage with switched capacitors. When the several capacitors and the input voltage sources are connected in parallel, the capacitors are charged. When the several capacitors and the input voltage sources are connected in series, the capacitors are discharged. The charge pump output the sum of the voltages of the capacitors and the input voltage sources. However, a charge pump has many switching devices which make the system more complicated.

In order to overcome the disadvantages of the conventional types of multilevel inverter and as a provision against the issue, a new boost switched capacitor multilevel inverter is implemented. A switched-capacitor (SC) inverter outputs multilevel voltages with switched capacitors. An SC inverter is similar to a charge pump in the topology. The new boost switched capacitor multilevel inverter can output larger voltage than the input voltage by switching the capacitors in series and in parallel. It makes use of only one dc source as the input and the numbers of switching devices are reduced when compared to the widely used conventional topologies. This multilevel inverter does not have any inductors which make the system small. The output harmonics of the novel multilevel inverter are reduced by the multilevel output. A block diagram of the circuit is given below to understand the entire structure of the system.

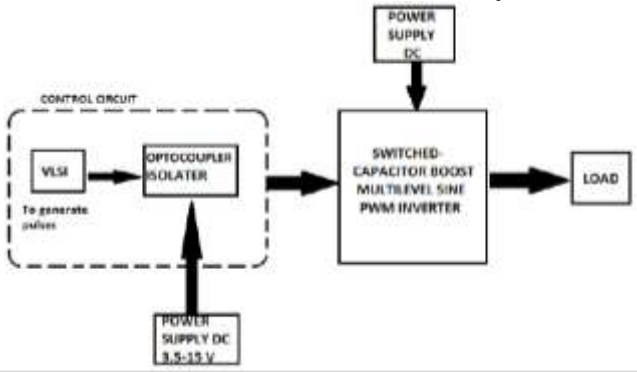

Fig. 1: Block diagram of the switched capacitor multilevel inverter system

II. SWITCHED CAPACITOR BOOSTED MULTILEVEL INVERTER

A new boost switched-capacitor (SC) multilevel inverter is formed by cascading two structures, a switched capacitor circuit and a two level (full bridge) inverter [6], [7], [8]. A switched capacitor circuit is a combination of capacitors, switching devices such as MOSFET, IGBT, BJT etc. One basic switched capacitor cell is formed by one capacitor, three switching devices with diodes. The switched capacitor circuit used here is sometimes regarded as Marx inverter. The novel multilevel inverter can be smaller than the conventional two stage inverter, which consists of boost converter and a full bridge inverter. Each of these cells are connected in parallel with each other to increases the number of levels that is desired in the multilevel output. Each of the cells is made to operate as a parallel-series converter, when two of the switches are simultaneously turn on, the capacitor comes in parallel with the source. These switches are turned off and an alternate switch is gated to make the charged capacitor to be in series with the input source. The proper switching of these devices is required for obtaining the desired output.

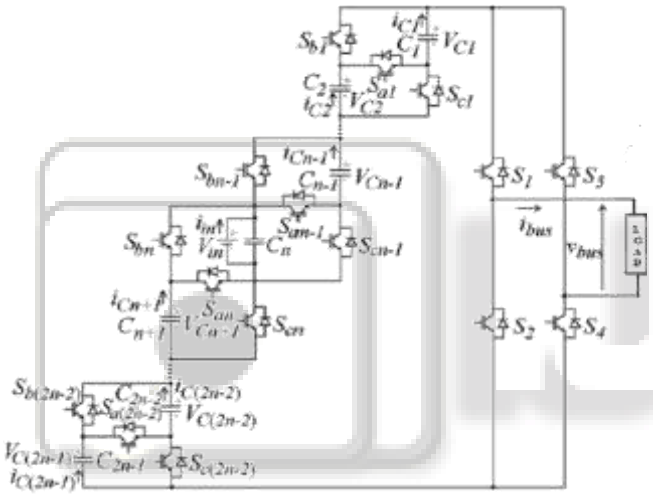

Fig. 2: circuit topology of switched capacitor multi-level inverter

A. Operating Modes of Switched Capacitor Multilevel Inverter

1) Mode 1(0 V)

All capacitors are made in parallel with the input source voltage, thus each capacitor maintains an input voltage across it. For this operation switches Sb_1; Sc_1; Sb_2; Sc_2 are ON. When the switches in the same side of the full bridge conduct and when there is no current flow in the capacitor. Switches in same upper/lower limb conduct that is either S_2; S_4 or S_1; S_3 are turned ON.

$$V_{bus} = 0 \text{ V}.$$

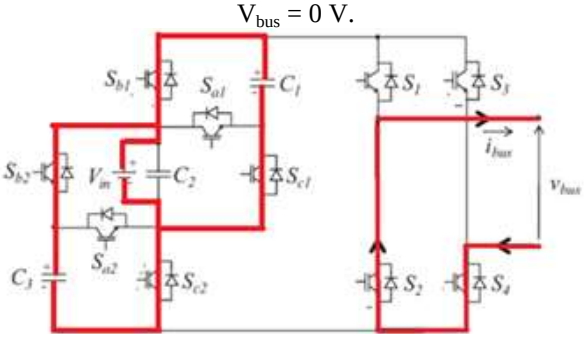

Fig. 3: Mode1 – 0V

2) Mode 2 ($V_{bus} = V_{in}$)

When all the capacitors are connected in parallel that is switches Sb_1; Sc_1; Sb_2; Sc_2 are ON and the switches S1 and S4 of full bridge inverter conducts. The bus voltage at this mode is given as,

$$V_{bus} = V_{in}$$

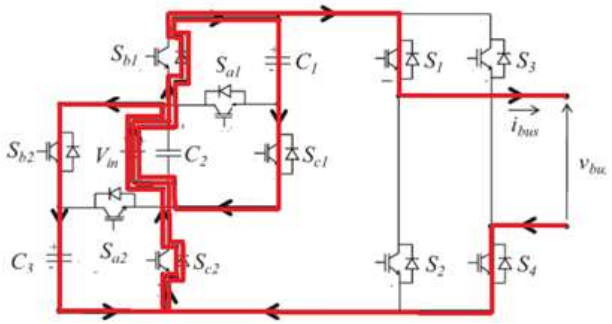

Fig. 4: Mode 2

3) Mode 3($V_{BUS} = 2V_{IN}$)

This is the mode when some of the capacitors are connected in series. The capacitor C_1 is connected in series with the source while the remaining capacitors are still in parallel with input voltage. This is obtained by switching off Sb_1, Sc1 and simultaneous turning ON of switch Sa_1. The switches Sb_2; Sc_2 are ON during this mode. The switches S_1 and S_4 of full bridge inverter are conducting in this period. The output voltage obtained is given as,

$$V_{bus} = V_{in} + V_{C1}$$

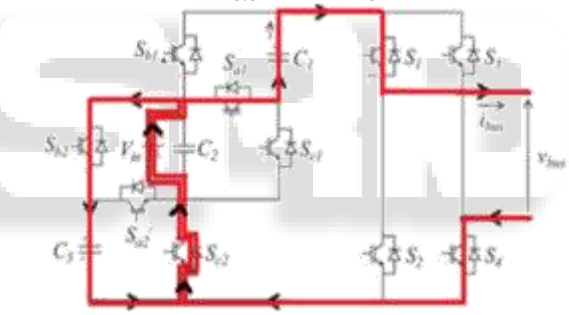

Fig. 5: mode 3

4) Mode 4 ($V_{bus} = 3V_{in}$)

In this mode all the capacitors are connected in series. The capacitor C1 and C2 are connected in series with the source voltage. This is obtained by switching off S_{b1}; S_{c1}; S_{b2}; S_{c2} and simultaneous turning ON of switches S_{a1} and S_{a2}. The switches

S_1 and S_4 of full bridge inverter are conducting in this period. The output voltage obtained is given as,

$$V_{bus} = V_{in} + V_{C1} + V_{C2}$$

Similarly the negative half cycle can be obtained by turning on S_2 and S_3 instead of S_1 and S_4, thus seven level output can be obtained.

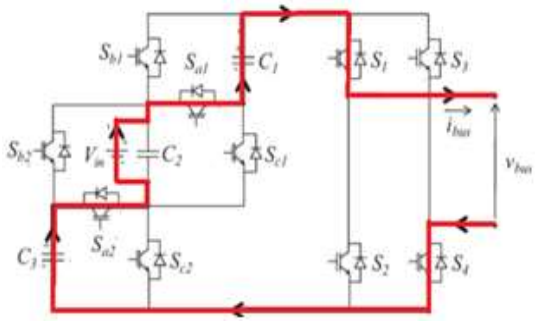

Fig. 6: mode 4

III. SIMULATION RESULTS

For an input of 5V, switching frequency f = 1.6 kHz and reference frequency = 50Hz , the multilevel inverter was simulated in Matlab Ra2010a. The capacitance C_k can be determined properly with considering the voltage ripple of the capacitors C_k. The smaller voltage ripple of these capacitors leads to the higher efficiency. The capacitance C_k are calculated when the maximum voltage ripple is supposed to be 10% of the maximum voltages of the capacitors. The capacitors C_k are charged when they are connected in parallel and are discharged when they are connected in series. The capacitor of 143 µF was used for 10% of maximum input voltage as voltage ripple.

A reference wave is compared with six triangular signals of same switching frequency based on the modulation index as the control strategy for obtaining the multilevel output. For a 7 level output, the modulation index is 3, the reference signals gets compared with all six of the carrier signal, the gate pulse thus produced will turn on switches such that only $V_{in,}$ $2V_{in}$ and $3V_{in}$ comes across as input to the inverter section. Figure 6.shows the output voltage which is 15V for an input of 5V and current can be seen below as 0.15A.

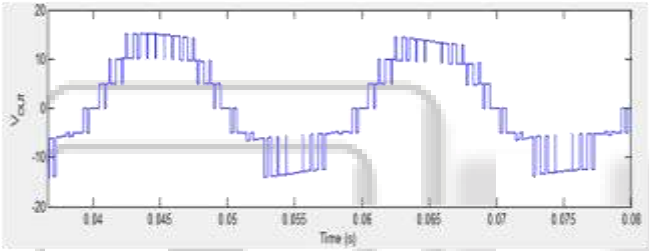

Fig. 6: M=3 output voltage

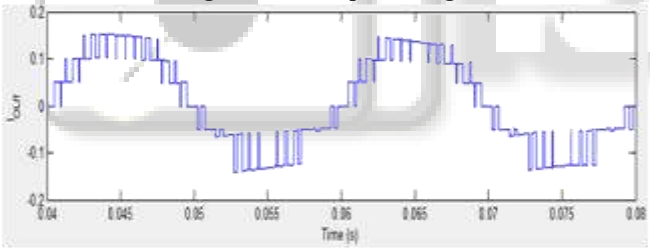

Fig. 7: M=3 output current

IV. EXPERIMENTAL SETUP AND RESULTS

The implementation of the prototype of Switched capacitor boost circuit requires to two main steps, first is the software implementation. Once the programming is done accurately for generating gate switching for switching devices, the hardware implementation of the circuit can be carried out. Software programming is done in VHDL language in ISE Xilinix design suite 14.1, its then downloaded to SPARTAN 3 kit. The switches used are MOSFET IFR540 along with its driver TLP250 which is an opto-coupler used to isolate and protect SPARTAN kit from any damage, and also to provide the required gating to turn on switches.

A. Software Implementation

The ISE design suite is used as the software for programming Spartan-3 kit. The 20 MHz system clock is used to generate a 50 Hz clock for sine wave and a 1.6 kHz clock for the triangular carrier waves. By using these clock signals sine signals and carrier signals are outed and each of the carriers are then compared. The gate pulses are obtained by performing logical operations on the compared signals obtained from the comparator. Below figure shows RTL schematic of the program, it can be seen that by using system clock gating signals are generated.

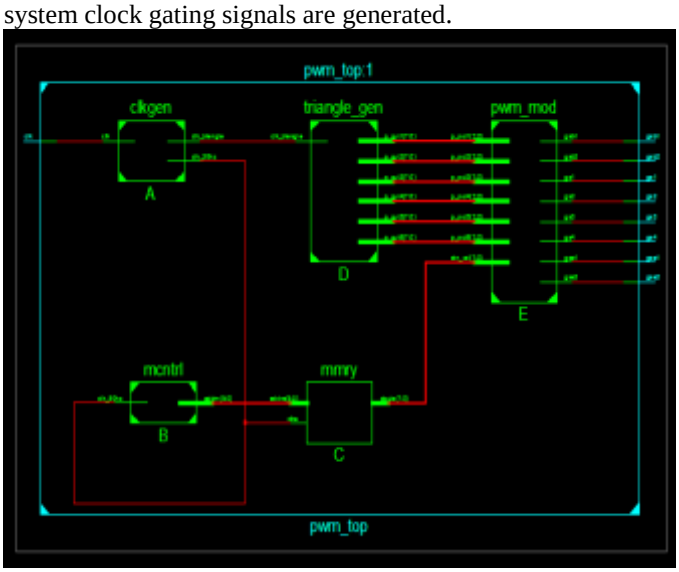

Fig. 8: RTL schematic

From the above figure it can be seen that the 50 Hz clock signal is given to two blocks. The first is the memory block, here a look up table is uploaded which contains 64 samples, each being of 8 bit size. The samples are taken such that we are able to generate a positive clamped sine wave with its starting at 127 instead of 0 and peak at 252. The second block is the memory control block, where address for outing each of the sample within the 50 Hz cycle is generated. The triangle-gen block is the one where 6 triangles are generated. These triangular waves are phase disposed with each of them having of 42 i.e. for the first triangle a counter starts at zero and reaches its maximum at 42nd count and then decreases to zero. Similarly for the second triangle it starts at 43 and reaches maximum at 42nd count and so on. Once the triangle signals are generated, each of them is compared with the sine wave, and various logical operations are performed to get the gate pulses.

B. Hardware Implementation

Once the software programming is over, it can be downloaded into the Spartan 3 kit by using a JTAG. This JTAG header consists of 0.1-inch stake pins and is located toward the top edge of the board. The Digilent low-cost parallel port to JTAG cable fits directly over the JTAG header stake pins. When properly fitted, the cable is perpendicular to the board, the signals at the end of the JTAG cable align with the labels listed on the board. The other end of the Digilent cable connects to the PCs parallel port. The Digilent cable is directly compatible with the Xilinx IMPACT software.

The downloaded program causes the logic arrays to be programmed and generate the required output signals. These output signals is then given to an opto-coupler isolator to prevent any feedbacks to the spartan kit as it can out only 3.3 V signals at a very small current. The opto-coupler is the driver for the MOSFET IRF540 used as switches in the prototype of the circuit as shown in figure below. Here two switched capacitor cells are connected in parallel, each cell is made of three switches and a capacitor.

This switched capacitor network is then connected to a full bridge inverter so as to obtain the desired output.

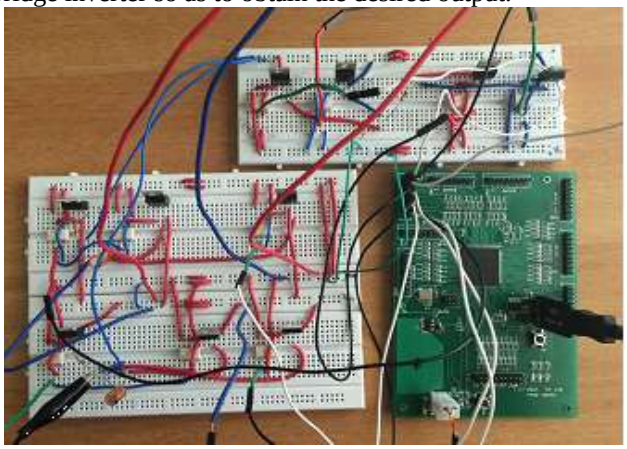

Fig. 9: Prototype of SC-MLI with Spartan 3 module

The below figures shows the gating pulses obtained from the FPGA, it can be seen that switches S_2 and S_4 conduct for a small time period so that the zero instant of sine is recreated. S_{b1} and S_{a1} are opposite signals, so is signals S_{b2} and S_{a2}. Switches S_{b1} and S_{c1} have same pulses and they operate simultaneously, so does switches S_{b2} and S_{c2}, they also conduct simultaneously.

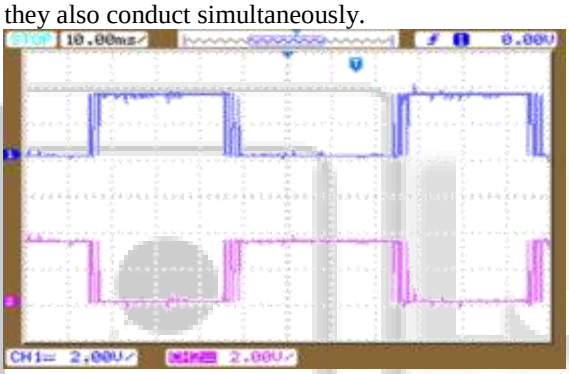

Fig. 10: gate pulse for S_1 and S_2

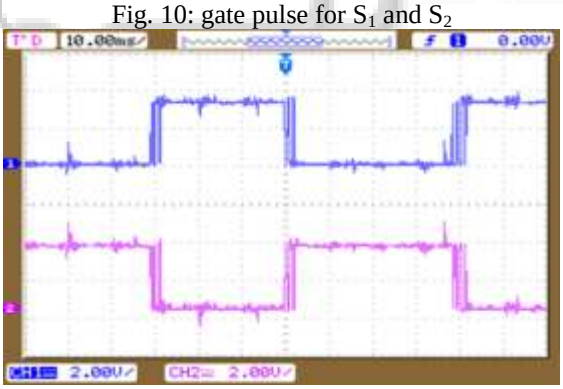

Fig. 11: gate pulse for S_3 and S_4

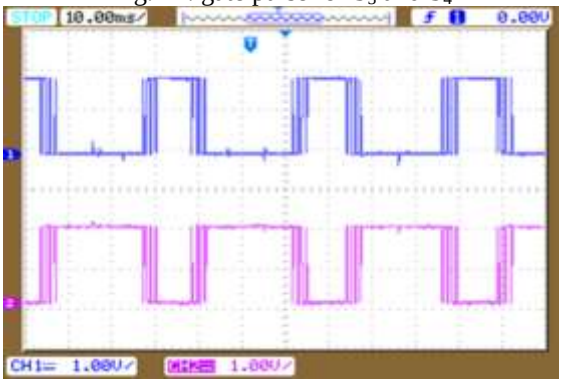

Fig. 12 gate pulse for S_{b1} and S_{a1}

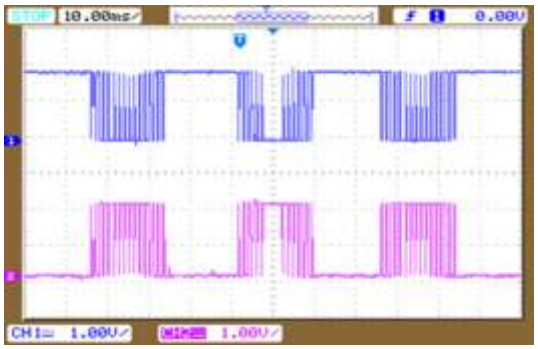

Fig. 13: gate pulse for S_{b2}, S_{a2}

The programming for obtaining a seven level output is performed in Xilinix software. When the above gate pulses are given to the prototype, a seven level output shown in the below figure is obtained. Here for an input of 1.2 V only an output of 2.9 V is obtained, even though by calculation it would have been 3.4V.

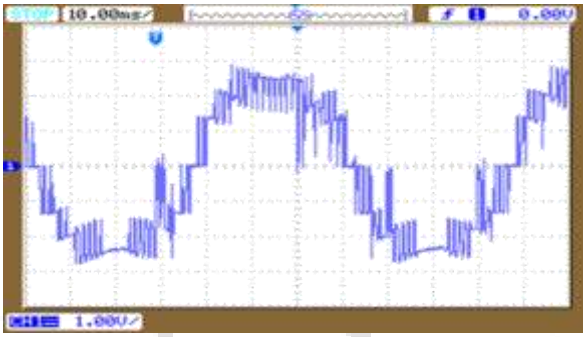

Fig. 14: Seven level SC-MLI output voltage

V. CONCLUSION

A new boost switched capacitor multilevel inverter was analyzed and it has much less number of switching devices when compared to the normally used topologies such as diode clamped, flying capacitor and cascaded H- bridge. Here only capacitors are used. The circuit is simulated in Matlab Ra2010a and it was seen that at each level the voltage increases that is it doubles, triples etc per level. Also it was seen by FFT analysis that % THD value decreases with increase in level. The total harmonic distortion was seen to be reduced to 25.65% for seven level output with 15 V as amplitude for an input of 5V.

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