

An Optimized Implementation of CSLA for 32-bit MAC using VHDL

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Abstract— This project deals with the comparison of the VLSI design of the carry select adder (CSLA) based 32-bit multiplier. Both the VLSI design of multiplier multiplies two 32-bit values and gives a product term of 64-bit values. The CLAA based multiplier uses the delay some time for performing multiplication operation where as in CSLA based multiplier also uses nearly the same delay time for multiplication operation. But the area needed for CLAA multiplier is reduced to 31 % by the CSLA based multiplier to complete the multiplication operation. With the growing importance of electronic products in day-to-day life, the need for portable electronic products with low power consumption largely increases. In this paper, Multiply Accumulator unit (MAC) with carry look-ahead adder (CLA) is being designed. In the same MAC architecture design in final adder stage of partial product unit the carry save adder (CSA), carry select adder (CSLA) are also used instead of CLA to compare the power and performance. These MAC designs were simulated and synthesized using Xilinx 13.2. These multipliers are implemented using Xilinx ISE, simulation diagrams are viewed through Xilinx ISE. The simulation result shows that the MAC design with CLA has area reducing by 15%, 35% reduction is seen in power analysis and 4times increase of delay analysis.

Key words: Low power, Multiplier and Accumulator, Carry Save Adder, Carry Look-ahead Adder, Carry Select Adder

I. INTRODUCTION

Now-a-days, there is a huge demand for portable electronic products. The electronic products with low power consumption like cellular mobiles, laptops and other portable communication devices would surely lead the market trend [1]. The MAC operation is the main computational operation in all digital designs. The speed of the processor mainly depends on the speed of the MAC unit. Development of high speed and low power MAC structure is thus very important for any real time processing application. The basic MAC structure consists of a partial product bit generation unit, a partial product bit compression unit and a final adder. Both the partial product reduction network and the accumulator unit require an addition operation that involves a long path for carry propagation. In the final addition operation of MAC structures, if carry propagation adder is used, the delay is increased. Since carry propagation is a time-consuming operation. To reduce this delay, a carry save adder is used instead of a carry propagation adder. But the power consumed by a carry save adder is equal to that of the carry propagation adder.

II. MULTIPLICATION ACCUMULATION UNIT

In computing, especially processing, the multiply-accumulate operation is a common step that computes the product of two numbers and adds that product to an accumulator. The hardware unit that performs the operation is known as a multiplier-accumulator (MAC, or

MAC unit); the operation itself is also often called a MAC or a MAC operation.

The function of the MAC unit is given by the following equation:

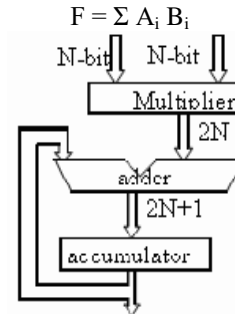


Fig. 1: Basic structure of MAC

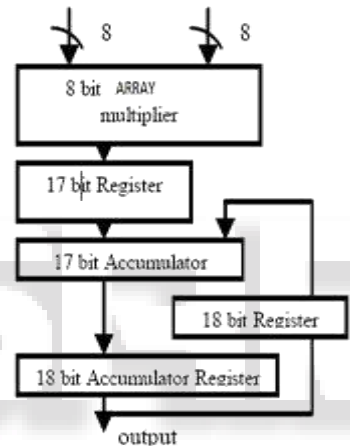


Fig. 2: MAC architecture

III. REVERSIBLE LOGIC GATE

It is an n-input n-output logic function in which there is a one-to-one correspondence between the inputs and the outputs. Because of this bijective mapping the input vector can be uniquely determined from the output vector. This prevents the loss of information which is the root cause of power dissipation in irreversible logic circuits.

A. Feynman Gate:

Feynman gate is a 2*2 one through reversible gate as shown in figure 1. The input vector is I(A, B) and the output vector is O(P, Q). The outputs are defined by P=A, Q=AB. Quantum cost of a Feynman gate is 1. Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs

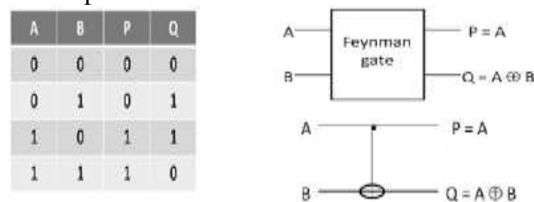


Fig. 3: Feynman Gate Figure & Truth Table

V. PERFORMANCE ANALYSIS

A. Area Analysis:

The performance analysis for the area of normal and reversible based MAC's are represented in the form of the diagram shown in figure below.

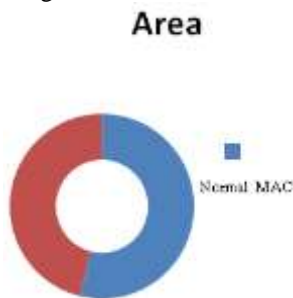


Fig. 9: Area Analysis Chart

Normal MAC	35925
Reversible logic MAC	30826

Table 1: Area Analysis

B. Delay Analysis:

The performance analysis for the delay of normal and reversible based MAC's are represented in the form of the diagram shown in figure below.

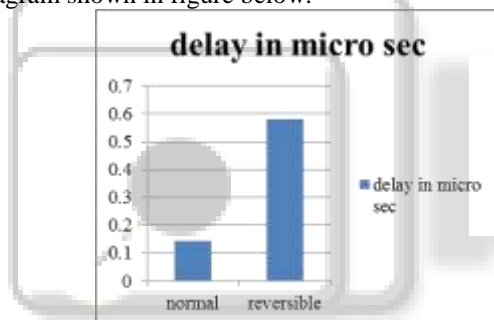


Fig. 10: Delay Analysis Chart

	Delay in Micro sec
Normal mac	0.143
Reversible mac	0.579

Table 2: Delay Analysis

C. Power Analysis:

1) Dynamic and Total Power Analysis in mw

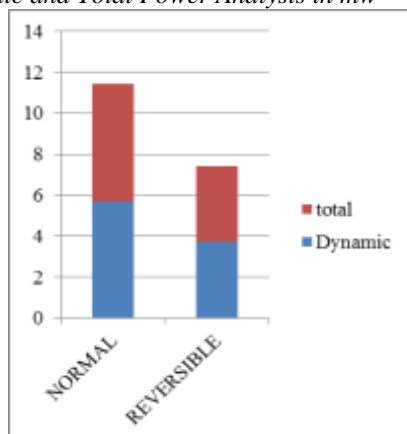


Fig. 11: Dynamic and Total Power Analysis in mw

2) Leakage Power Analysis in nw

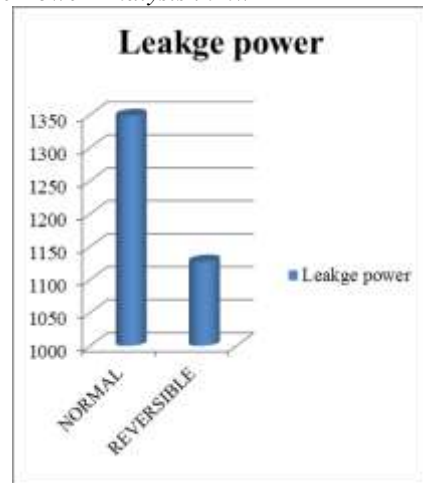


Fig. 12: Leakage Power Analysis in nw

The power performance analyses for the normal and reversible based MAC's are represented in the form of the diagram shown in figure and the table above.

VI. CONCLUSION

A design and performance of a DIGITAL CADENCE-based MAC both with NORMAL and REVERSIBLE was presented. HDL was used to simulate our MAC's. Digital cadence was used to synthesis the area, delay, power. Using REVERSIBLE improves the performance of the MAC's in terms of area and power.

The following are can be concluded from the analysis of reversible logic MAC and Normal MAC

- There is a 15% reduction is seen in area analysis of MAC.
- There is a 35% reduction is seen in power analysis of MAC.
- There is a 4times increase of delay analysis of MAC.

Thus we can say Reversible logic MAC is better in terms of area and power.

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